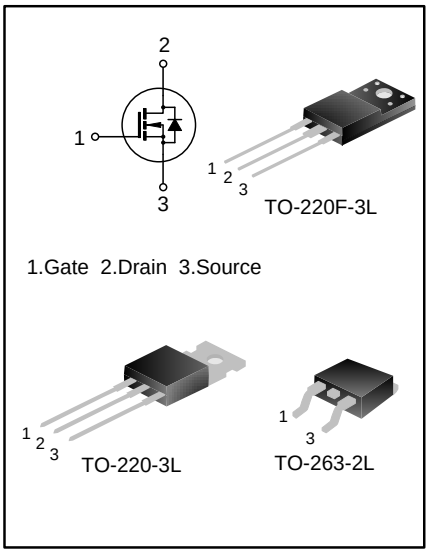
8A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD840T/F/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 8A, 500V, $R_{DS(on)(typ.)}$=0.62Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVD840T	TO-220-3L	SVD840T	Pb free	Tube
SVD840F	TO-220F-3L	SVD840F	Pb free	Tube
SVD840S	TO-263-2L	SVD840S	Halogen free	Tube
SVD840STR	TO-263-2L	SVD840S	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Rating			Unit
			SVD840T	SVD840F	SVD840S	
Drain-Source Voltage		V_{DS}	500			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	8.0			A
	T_C=100°C		5.1			
Drain Current Pulsed		I_{DM}	32			A
Power Dissipation(T_C=25°C)		P_D	135	49	126	W
-Derate above 25°C			1.08	0.39	1.01	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	686			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating			Unit
		SVD840T	SVD840F	SVD840S	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.93	2.56	0.99	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.0A	--	0.62	0.9	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	1186	--	pF
Output Capacitance	C_{oss}		--	116	--	
Reverse Transfer Capacitance	C_{rss}		--	11	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V, I_D=8.0A, R_G=25Ω (Note 2,3)	--	16	--	ns
Turn-on Rise Time	t_r		--	33	--	
Turn-off Delay Time	$t_{d(off)}$		--	79	--	
Turn-off Fall Time	t_f		--	35	--	
Total Gate Charge	Q_g	V_{DS}=400V, I_D=8.0A, V_{GS}=10V (Note 2,3)	--	31	--	nC
Gate-Source Charge	Q_{gs}		--	5.6	--	
Gate-Drain Charge	Q_{gd}		--	12	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	8.0	A
Pulsed Source Current	I_{SM}		--	--	32	
Diode Forward Voltage	V_{SD}	I_S=8.0A, V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	I_S=8.0A, V_{GS}=0V, dI_F/dt=100A/μS (Note 2)	--	270	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.89	--	μC

Notes:

1. L=30mH, I_{AS}=5.76A, V_{DD}=188V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

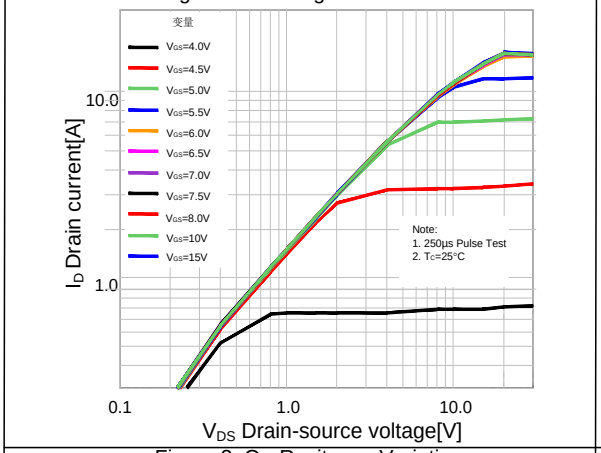


Figure 2. Transfer Characteristics

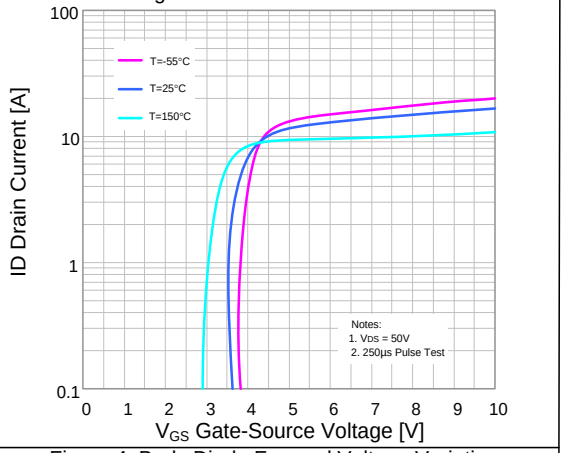


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

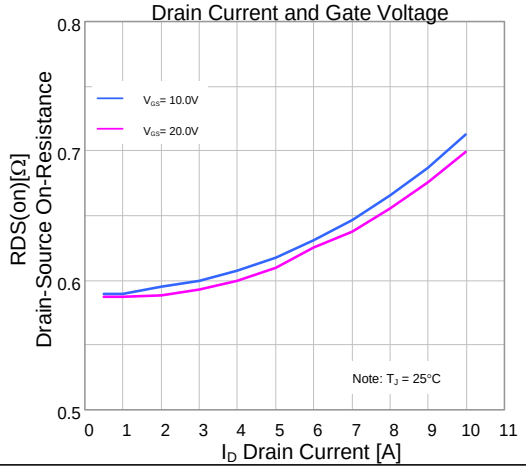


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

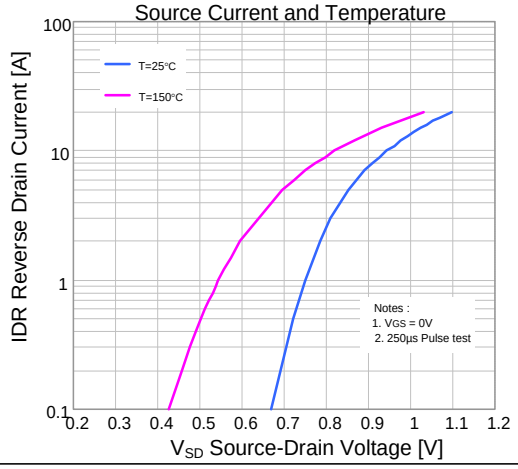


Figure 5. Capacitance Characteristics

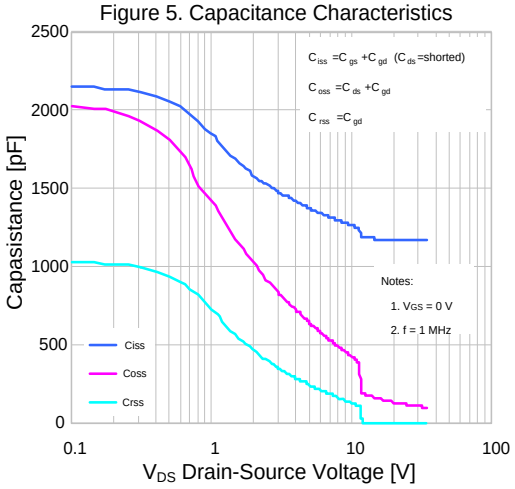
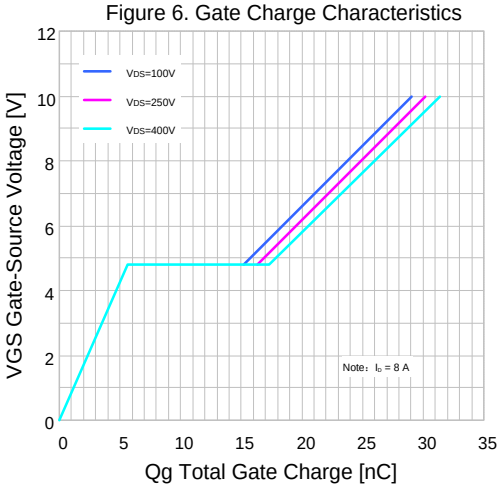


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

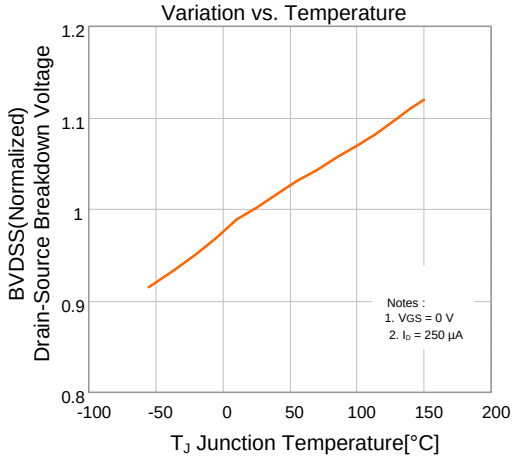


Figure 8. On-resistance Variation vs Temperature

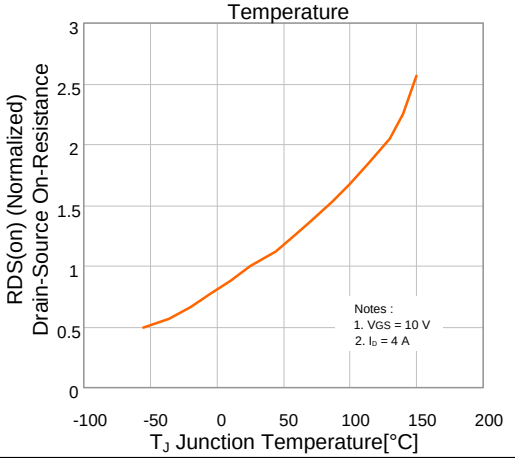


Figure 9-1. Max. Safe Operating Area(SVD840T)

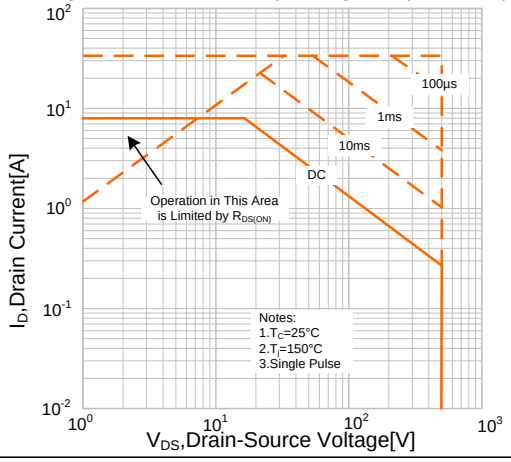


Figure 9-2. Max. Safe Operating Area(SVD840F)

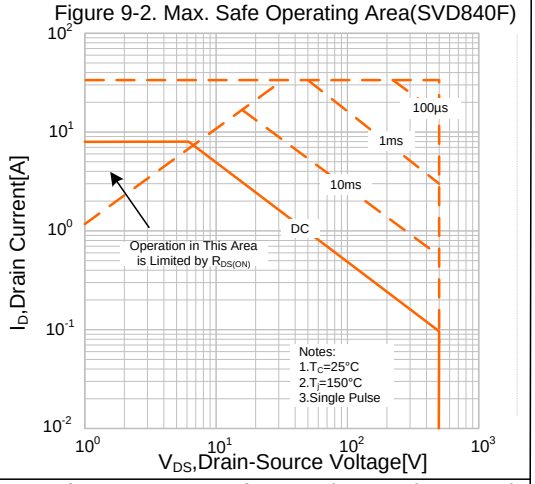


Figure 9-1. Max. Safe Operating Area(SVD840T)

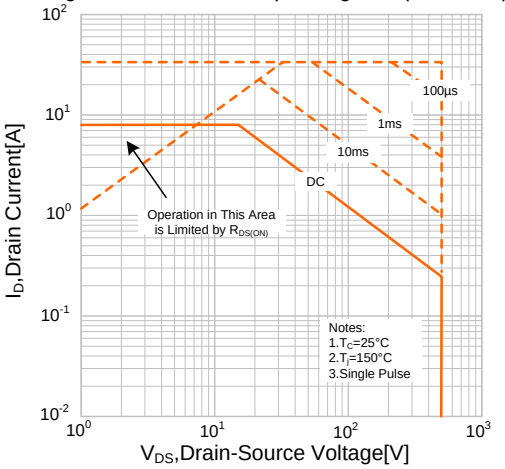
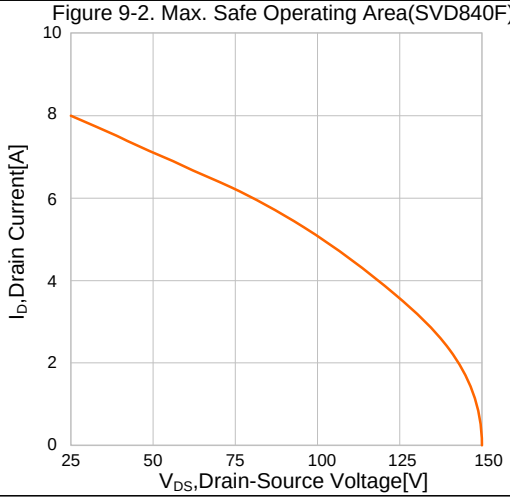
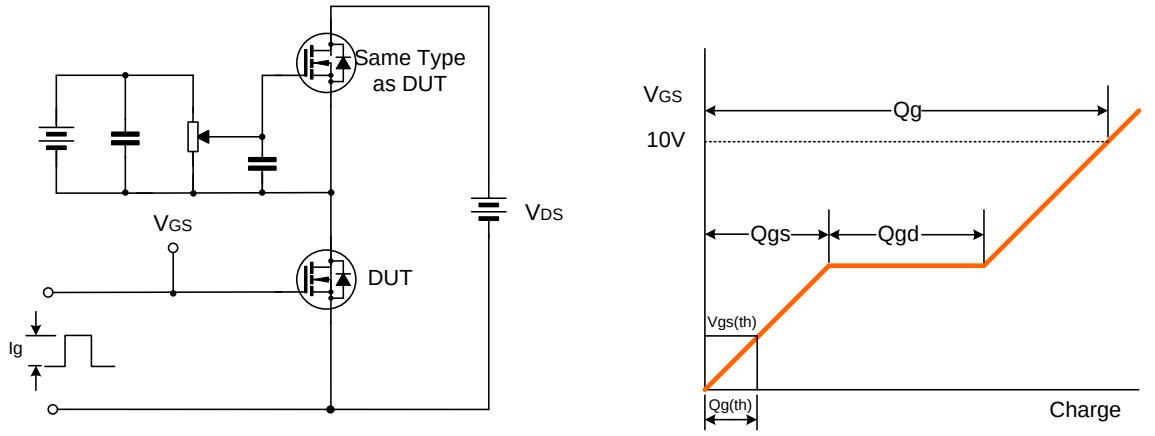


Figure 9-2. Max. Safe Operating Area(SVD840F)

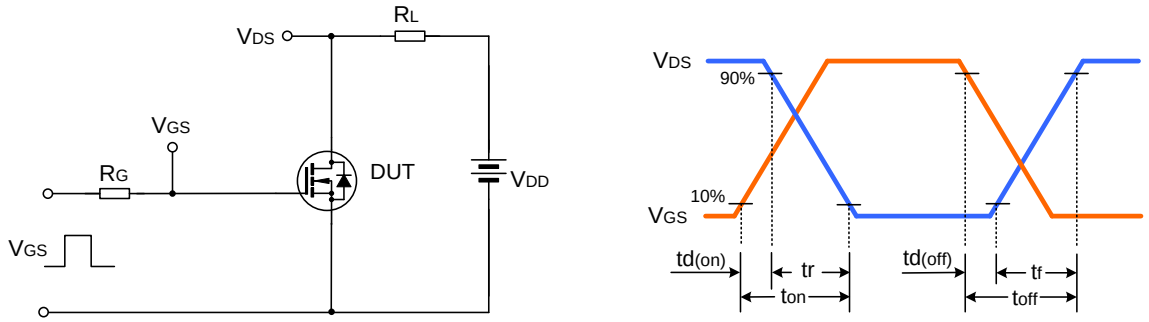


TYPICAL TEST CIRCUIT

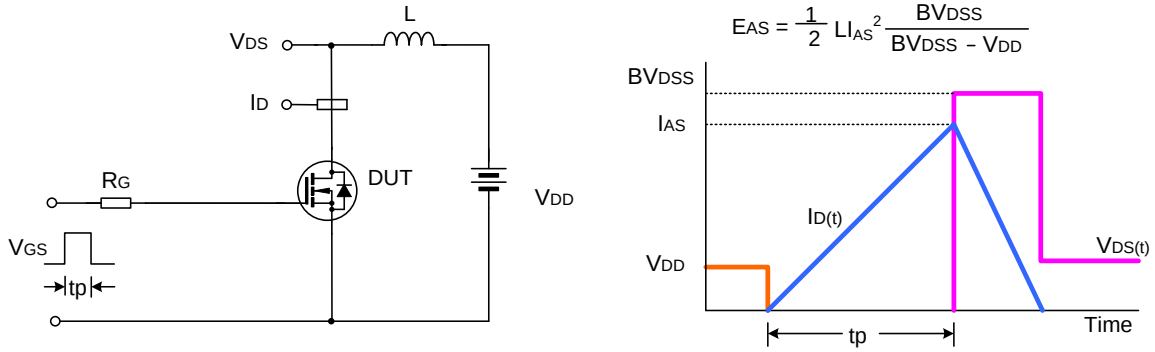
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

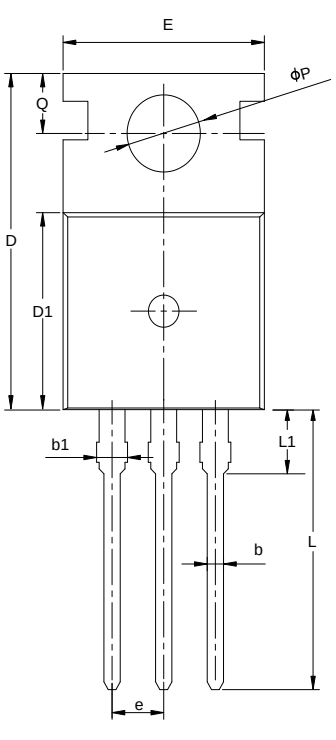


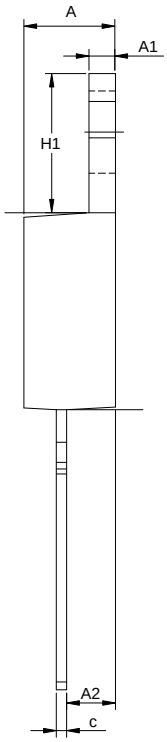
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

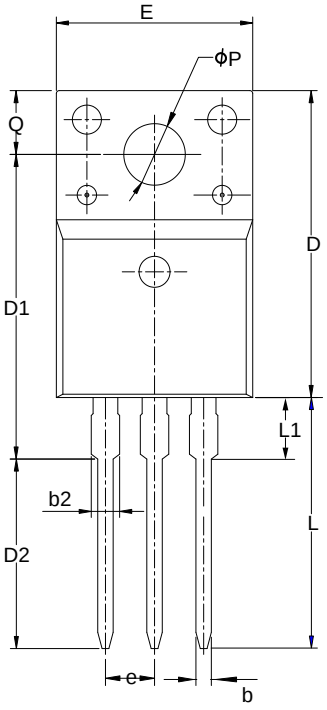
TO-220-3L **UNIT: mm**

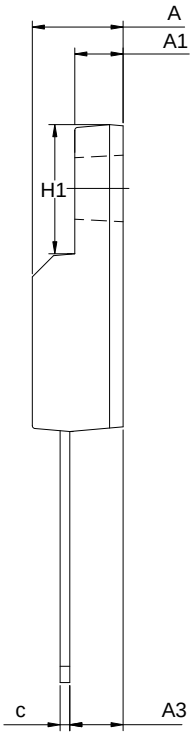




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-220F-3L **UNIT: mm**

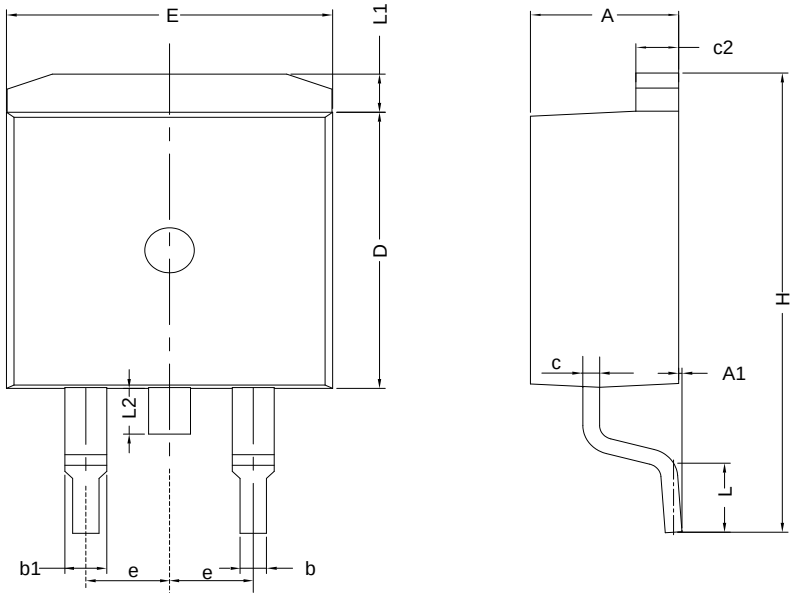




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE (CONTINUED)

TO-263-2L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
b1	1.17	—	1.50
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

Important notice:

1. **The instructions are subject to change without notice!**
2. **Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.**
3. **Our products are consumer electronic products or the other civil electronic products.**
4. **When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.**
5. **It is strongly recommended to identify the trademark when buying our products. Please contact us if there is any question.**
6. **Product promotion is endless, our company will wholeheartedly provide customers with better products!**
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Rev.: 2.2
Revision History:
1. Update Turn-on/off time
2. Update typical test circuit
3. Update important notice
4. Update package outlinne

Rev.: 2.1
Revision History:
1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-220-3L

Rev.: 2.0
Revision History:
1. Modify the thermal characteristics

Rev.: 1.9
Revision History:
1. Add the package of TO-263-2L

Rev.: 1.8
Revision History:
1. Modify the ordering information

Rev.: 1.7
Revision History:
1. Change the schematic diagram of MOS

Rev.: 1.6
Revision History:
1. Modify “ELECTRICAL CHARACTERISTICS” and the capacitance characteristic curve

Rev.: 1.5
Revision History:
1. Modify “PACKAGE OUTLINE”

Rev.: 1.4
Revision History:
1. Modify “PACKAGE OUTLINE”

Rev.: 1.3
Revision History:
1. Modify the template of Datasheet

Rev.: 1.2
Revision History:
1. Modify ”TYPICAL CHARACTERISTICS”

Rev.: 1.1
Revision History:
1. Modify the value of PD, Thermal Resistance, Junction-to-Case
2. Add SOA and ID-TC

Rev.: 1.0
Revision History:
1. First release