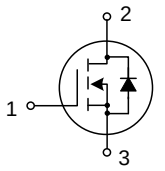
14A, 650V N-CHANNEL MOSFET

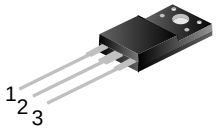
GENERAL DESCRIPTION

The SVFP14N65CFJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



1.Gate 2.Drain 3.Source



TO-220FJ-3L

FEATURES

- 14A, 650V, $R_{DS(on)(typ.)}$= 0. 6Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE

S V F P X N E X X C X

Silan VDMOS Code of F-Cell process

Process Version,P denotesPASSIVATION

Nominal current,using 1 or 2 digits: Example:4 denotes 4A,10 denotes 10A,08 denotes 0.8A

N denotes N Channel

Package information. Example: FJ:TO-220FJ;FQ:TO-220FQ

REV.

Nominal Voltage,using 2 digits Example: 60 denotes 600V, 65 denotes 650V.

Special Features indication, May be omitted. Example: E denotes embeded ESD structure

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVFP14N65CFJ	TO-220FJ-3L	P14N65CFJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	14	A
	T_C=100°C		11	
Drain Current Pulsed		I_{DM}	56	A
Power Dissipation(T_C=25°C)		P_D	45	W
- Derate above 25°C			0.36	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	820	mJ
Operation Junction Temperature Rating		T_J	-55～+150	°C
Storage Temperature Rating		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.78	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V，I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V，V_{GS}=0V	--	--	200	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V，V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}，I_D=250μA	2.0	--	4.0	V
On State Resistance	$R_{DS(on)}$	V_{GS}=10V，I_D=7.0A	--	0.60	0.70	Ω
Input Capacitance	C_{iss}	V_{DS}=25V，V_{GS}=0V，f=1.0MHz	--	1670	--	pF
Output Capacitance	C_{oss}		--	169	--	
Reverse Transfer Capacitance	C_{rss}		--	6.2	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V，I_D=14A，R_G=24Ω (Note 2,3)	--	29.27	--	ns
Turn-on Rise Time	t_r		--	44.07	--	
Turn-off Delay Time	$t_{d(off)}$		--	69.73	--	
Turn-off Fall Time	t_f		--	39.87	--	
Total Gate Charge	Q_g	V_{DS}=520V，I_D=14A，V_{GS}=10V (Note 2,3)	--	28.43	--	nC
Gate-Source Charge	Q_{gs}		--	9.79	--	
Gate-Drain Charge	Q_{gd}		--	7.92	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	14	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	56	
Diode Forward Voltage	V_{SD}	I_S=14A, V_{GS}=0V	--	--	1.2	V
Reverse Recovery Time	T_{rr}	I_S=14A, V_{GS}=0V,	--	573.69	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μS (Note 2)	--	6.01	--	μC

Notes:

1. L=30mH, I_{AS}=6.66A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

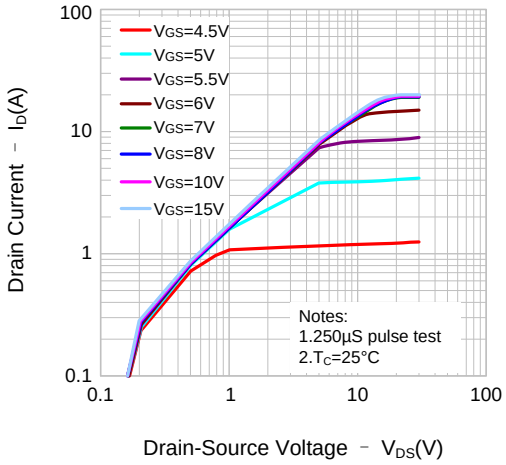


Figure 2. Transfer Characteristics

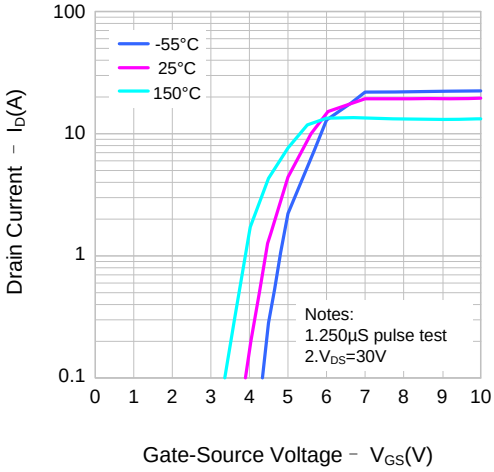


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

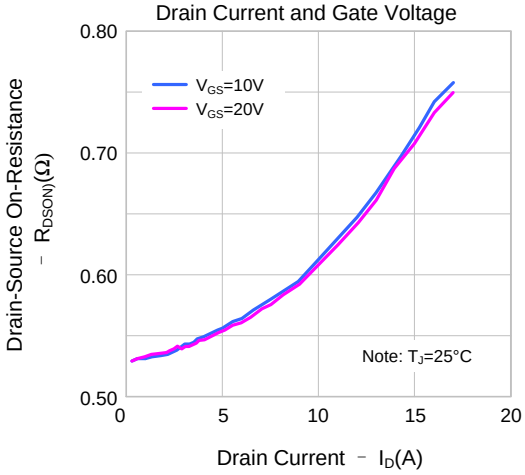


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

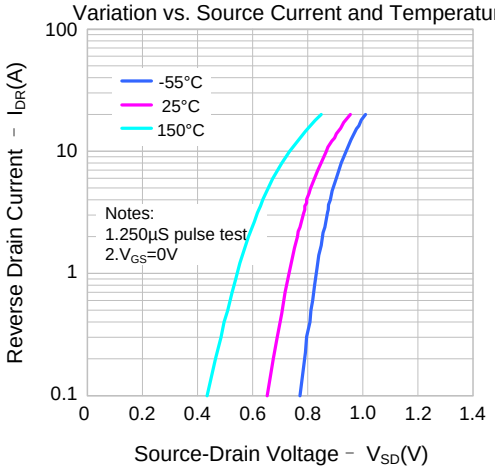


Figure 5. Capacitance Characteristics

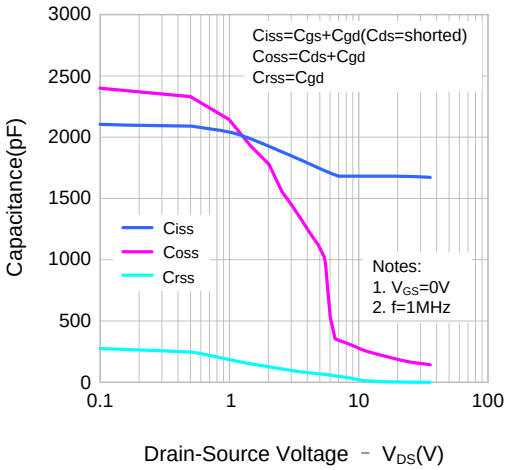
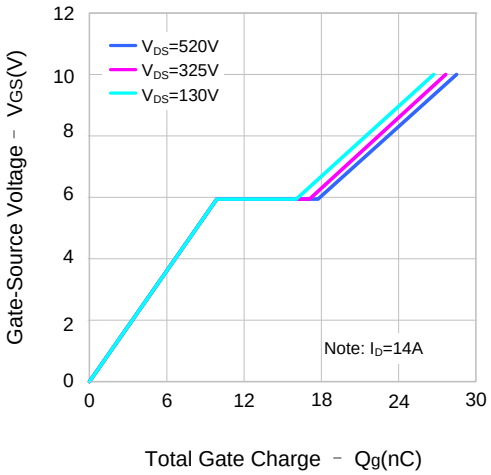


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

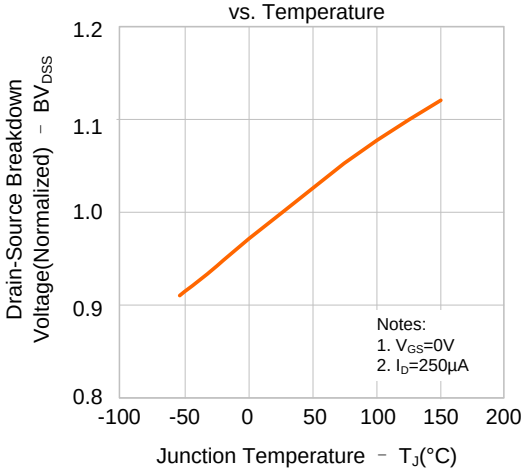


Figure 8. On-resistance Variation vs. Temperature

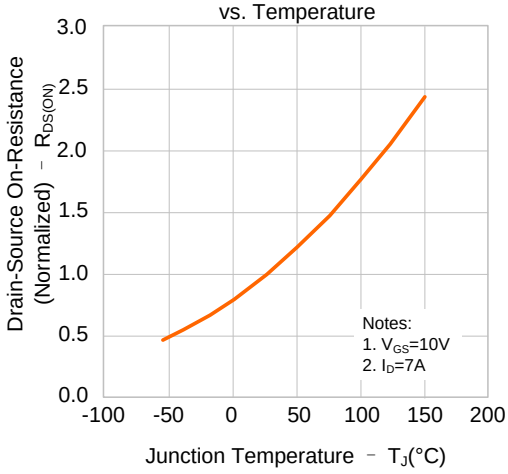


Figure 9. Max. Safe Operating Area

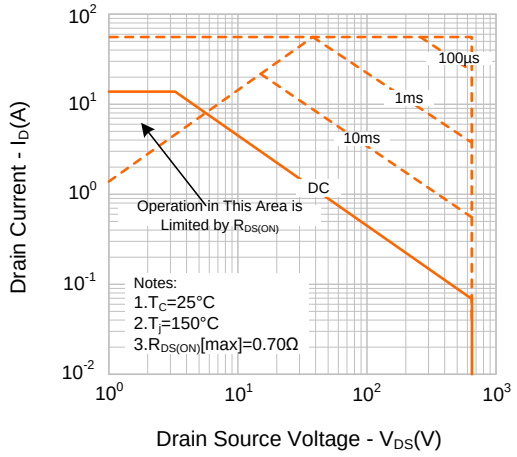
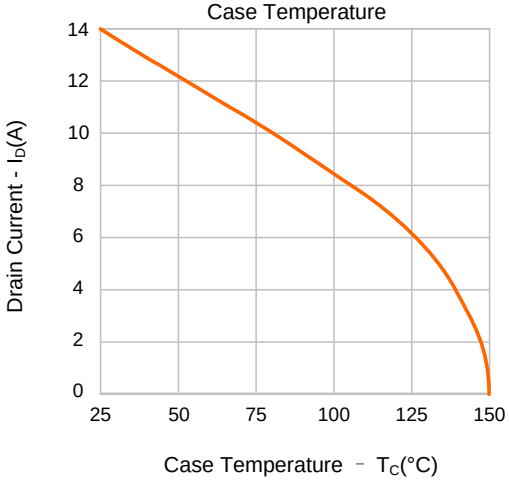
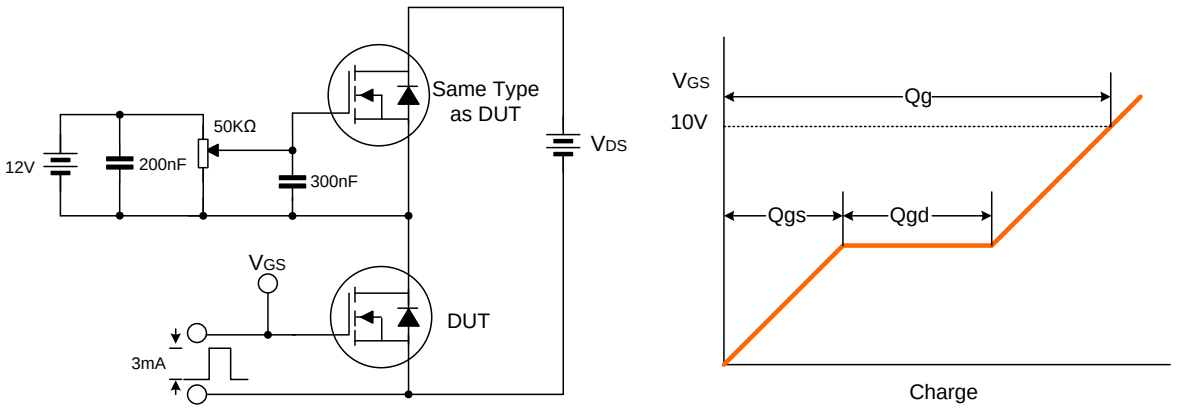


Figure 10. Maximum Drain Current vs. Case Temperature

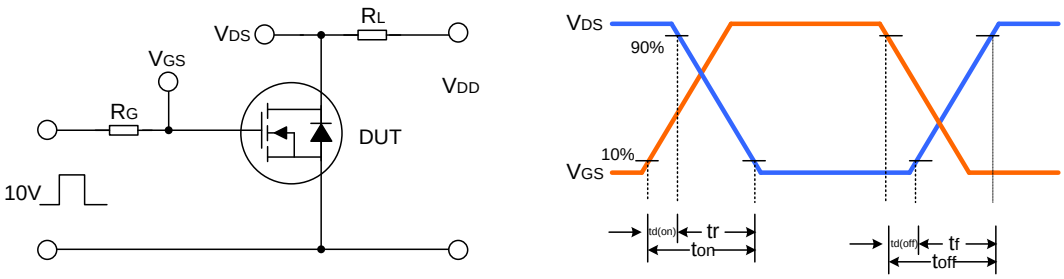


TYPICAL TEST CIRCUIT

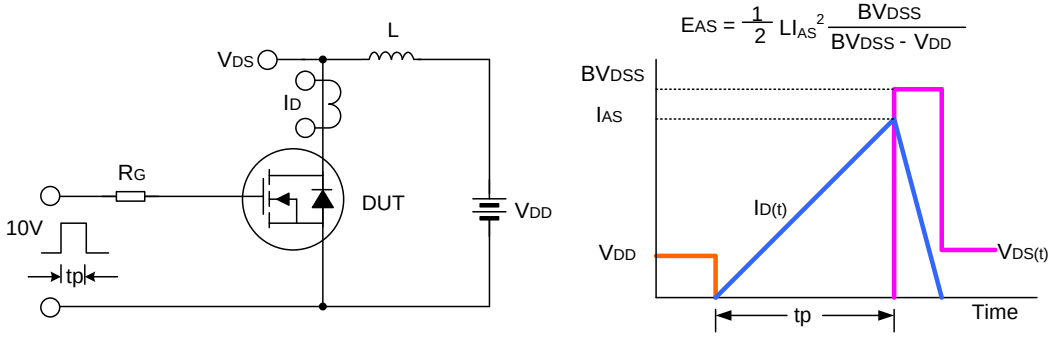
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

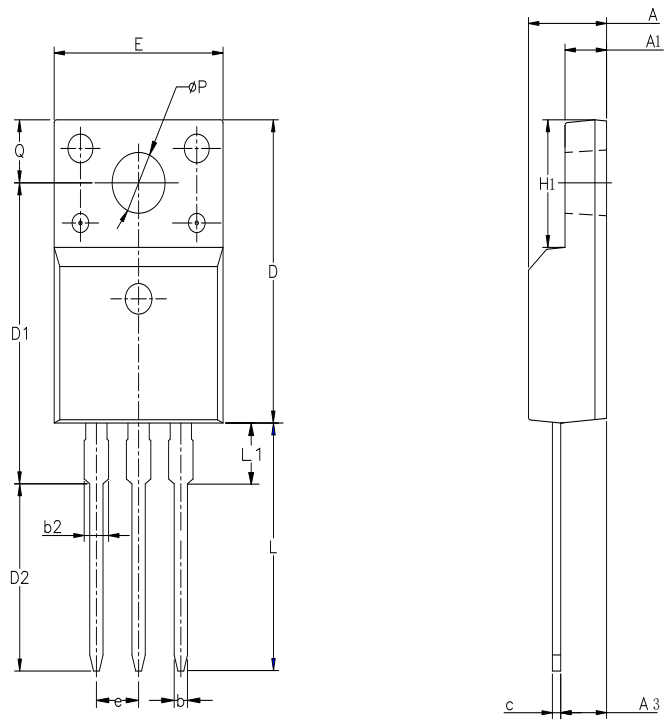


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 1.1

Revision History:

1. Modify values of I_{DSS} and V_{SD}

Rev.: 1.0

Revision History:

1. First Release