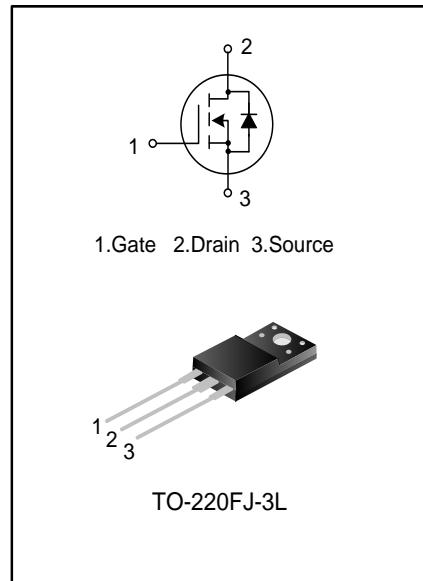


## 6A, 650V N-CHANNEL MOSFET

### GENERAL DESCRIPTION

SVF6N65VFJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

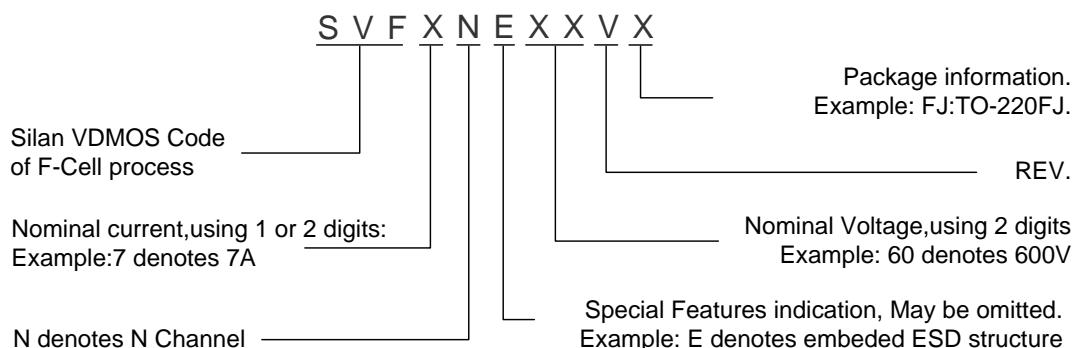
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



### FEATURES

- 6A, 650V,  $R_{DS(on)(typ.)}=0.80\Omega @ V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF6N65VFJ	TO-220FJ-3L	SVF6N65VFJ	Halogen free	Tube



## ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		$V_{DS}$	650	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	V
Drain Current	$T_c = 25^\circ\text{C}$	$I_D$	6	A
	$T_c = 100^\circ\text{C}$		3.8	
Drain Current Pulsed		$I_{DM}$	24	A
Power Dissipation( $T_c=25^\circ\text{C}$ ) -Derate above $25^\circ\text{C}$		$P_D$	50	W
			0.4	$\text{W}/^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)		$E_{AS}$	618	mJ
Operation Junction Temperature Range		$T_J$	-55~+150	$^\circ\text{C}$
Storage Temperature Range		$T_{stg}$	-55~+150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=650\text{V}$ , $V_{GS}=0\text{V}$	--	--	1.0	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30\text{V}$ , $V_{DS}=0\text{V}$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{GS}=V_{DS}$ , $I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$ , $I_D=5.0\text{A}$	--	0.8	1.0	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$	--	1159	--	pF
Output Capacitance	$C_{oss}$		--	126	--	
Reverse Transfer Capacitance	$C_{rss}$		--	11.3	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325\text{V}$ , $I_D=6\text{A}$ , $R_G=24\Omega$ (Note 2,3)	--	20.3	--	ns
Turn-on Rise Time	$t_r$		--	31.9	--	
Turn-off Delay Time	$t_{d(off)}$		--	79.6	--	
Turn-off Fall Time	$t_f$		--	34.9	--	
Total Gate Charge	$Q_g$	$V_{DS}=520\text{V}$ , $I_D=6\text{A}$ , $V_{GS}=10\text{V}$ (Note 2,3)	--	29.6	--	nC
Gate-Source Charge	$Q_{gs}$		--	7.5	--	
Gate-Drain Charge	$Q_{gd}$		--	12.5	--	



## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse p-n Junction Diode in the MOSFET	--	--	6	A
Pulsed Source Current	$I_{SM}$		--	--	24	
Diode Forward Voltage	$V_{SD}$	$I_S=6A, V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	$T_{rr}$	$I_S=6A, V_{GS}=0V,$ $dI_F/dt=100A/\mu s$	--	456.7	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	2.9	--	$\mu C$

**Notes:**

1.  $L=30mH, I_{AS}=6.0A, V_{DD}=100V, R_G=25\Omega, \text{starting } T_J=25^\circ C;$
2. Pulse Test: Pulse width  $\leq 300\mu s, \text{Duty cycle} \leq 2\%;$
3. Essentially independent of operating temperature.

## TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

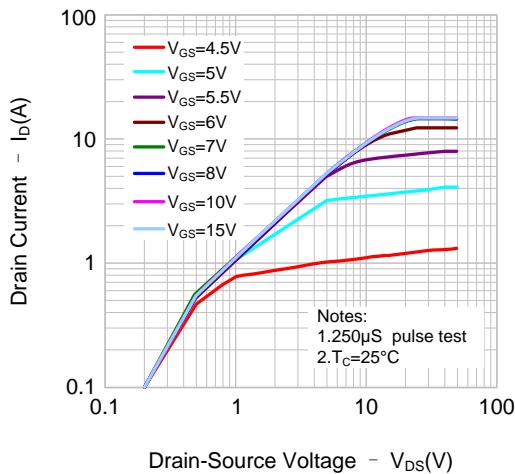


Figure 2. Transfer Characteristics

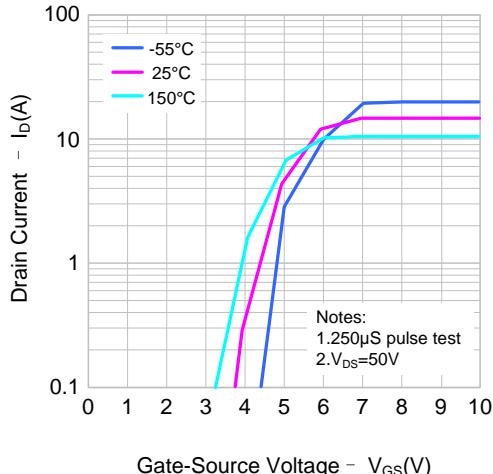


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

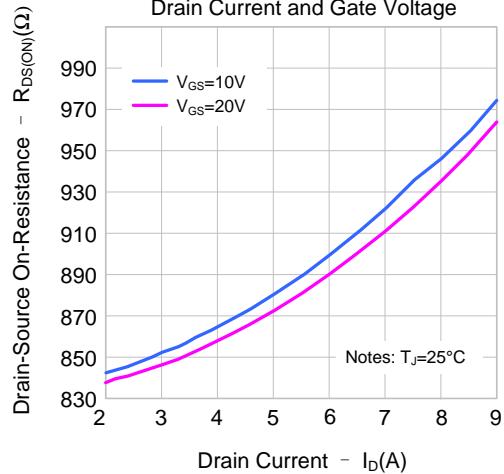
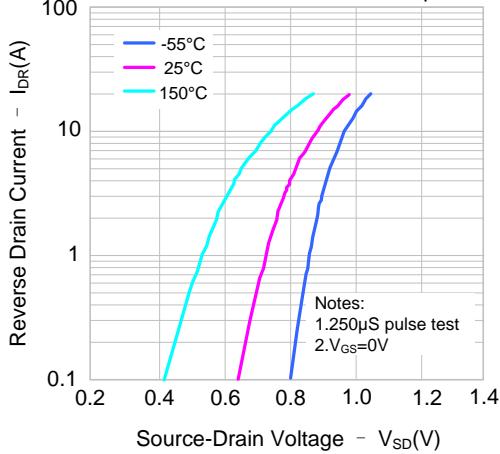


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature





## TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

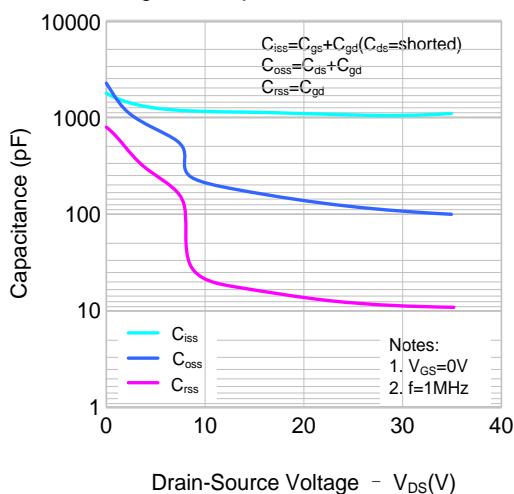


Figure 6. Gate Charge Characteristics

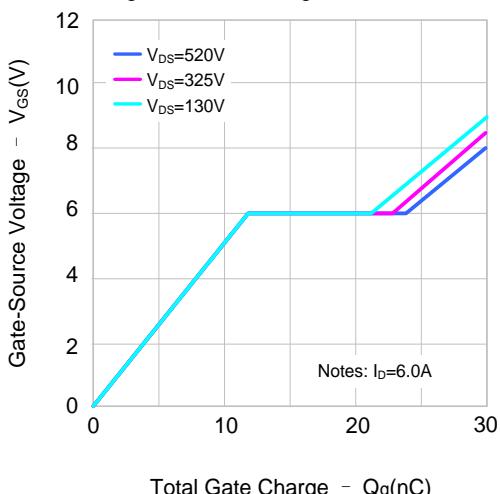


Figure 7. Breakdown Voltage Variation vs. Temperature

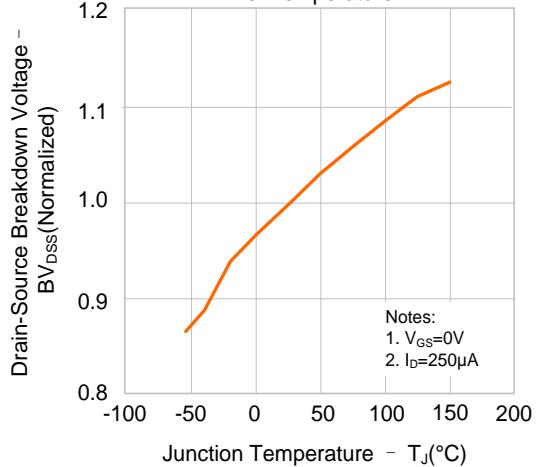


Figure 8. On-resistance vs. Temperature

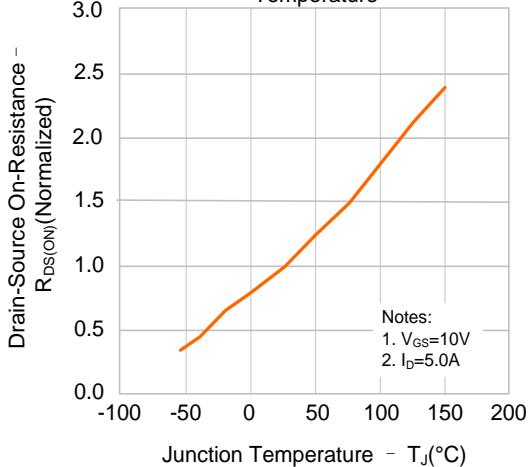


Figure 9. Max. Safe Operating Area

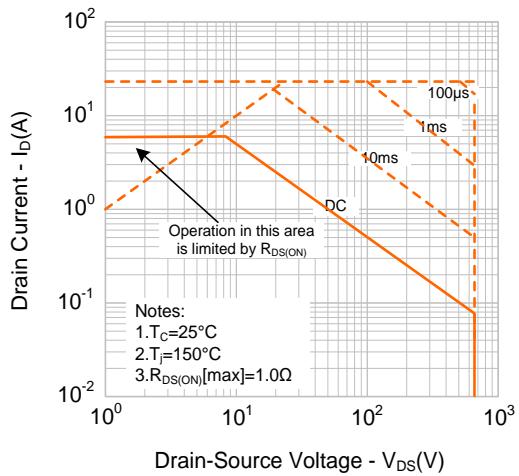
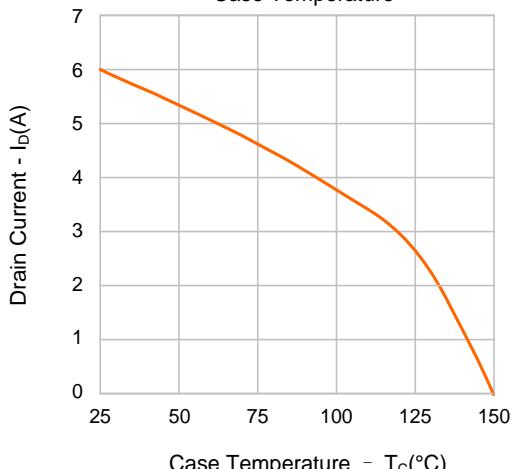


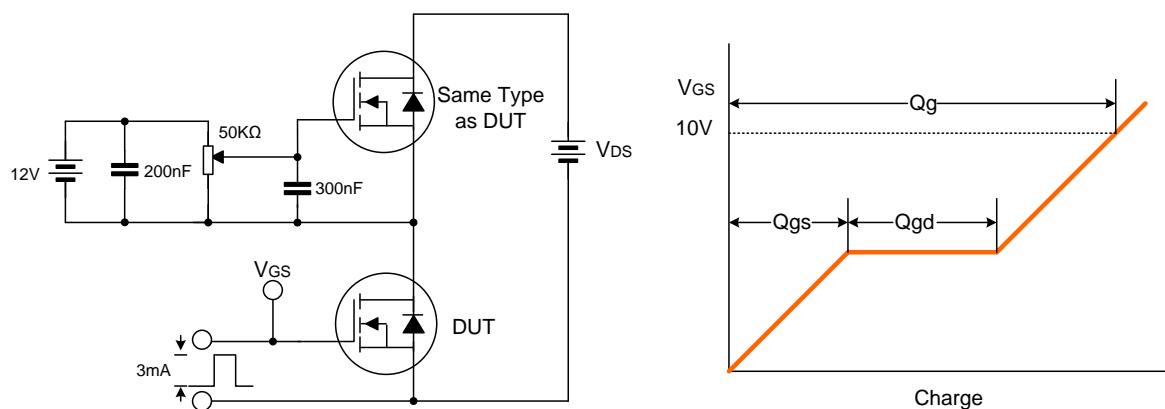
Figure 10. Max. Drain Current vs. Case Temperature



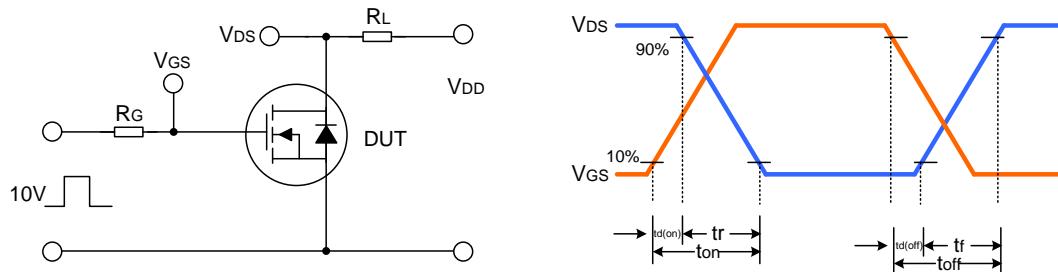


## TYPICAL TEST CIRCUIT

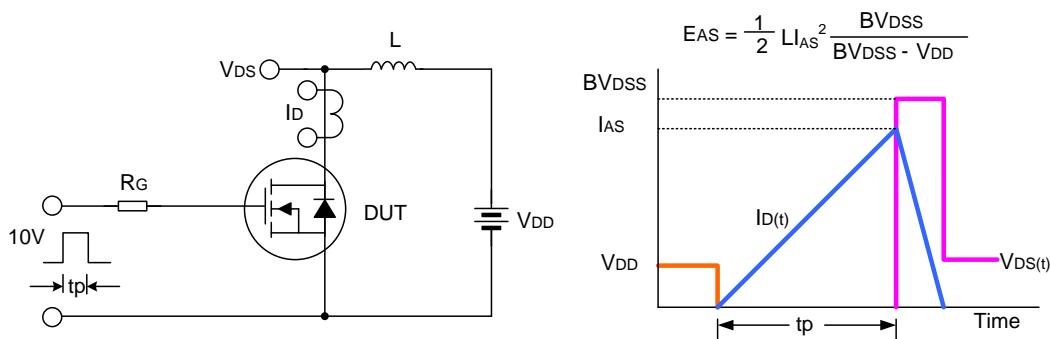
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



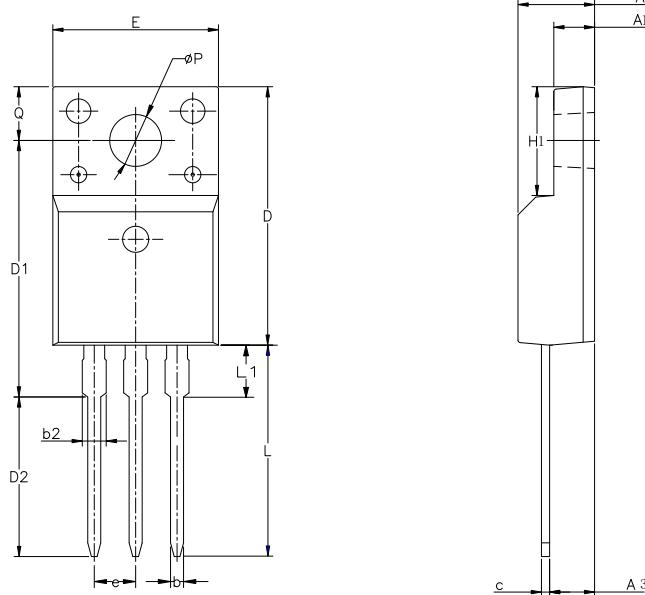
Unclamped Inductive Switching Test Circuit & Waveform



## PACKAGE OUTLINE

TO-220FJ-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 1.1

Revision History:

1. Modify Electrical characteristics
- 

Rev.: 1.0

Revision History:

1. First release
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