

6A, 800V N-CHANNEL MOSFET

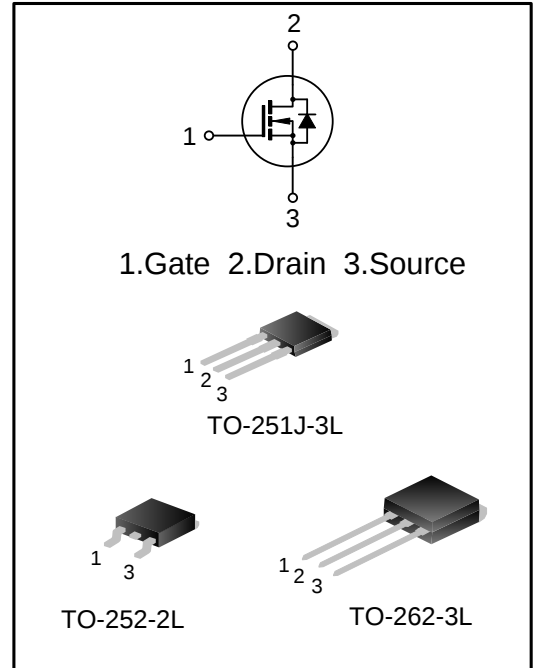
GENERAL DESCRIPTION

SVF6N80D(K)(MJ) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 6A,800V, $R_{DS(on)(typ.)}=2.0\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF6N80DTR	TO-252-2L	SVF6N80D	Halogen free	Tape&Reel
SVF6N80K	TO-262-3L	SVF6N80K	Pb free	Tube
SVF6N80MJ	TO-251J-3L	SVF6N80MJ	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings		Unit
			SVF6N80D/MJ	SVF6N80K	
Drain-Source Voltage		V _{DS}	800		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	6.0		A
	T _C =100°C		3.9		
Drain Current Pulsed		I _{DM}	24		A
Power Dissipation(T _C =25°C)		P _D	132	138	W
-Derate above 25°C			1.06	1.1	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	323		mJ
Reverse Diode dv/dt (Note 2)		dv/dt	4.5		V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF6N80D/MJ	SVF6N80K	
Thermal Resistance, Junction-to-Case	R _{θJC}	0.95	0.91	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	800	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =800V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.0A	--	2.0	2.7	Ω
Input Capacitance	R _g	f=1.0MHz	--	4.8	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	---	677	---	pF
Output Capacitance	C _{oss}		--	71	--	
Reverse Transfer Capacitance	C _{rss}		--	4.0	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =400V, I _D =6.0A, R _G =25Ω (Note 3,4)	--	12	--	ns
Turn-on Rise Time	t _r		--	23	--	
Turn-off Delay Time	t _{d(off)}		--	25	--	
Turn-off Fall Time	t _f		--	23	--	
Total Gate Charge	Q _g	V _{DS} =640V, I _D =6.0A, V _{GS} =10V (Note 3,4)	--	15	--	nC
Gate-Source Charge	Q _{gs}		--	4.3	--	
Gate-Drain Charge	Q _{gd}		--	6.8	--	

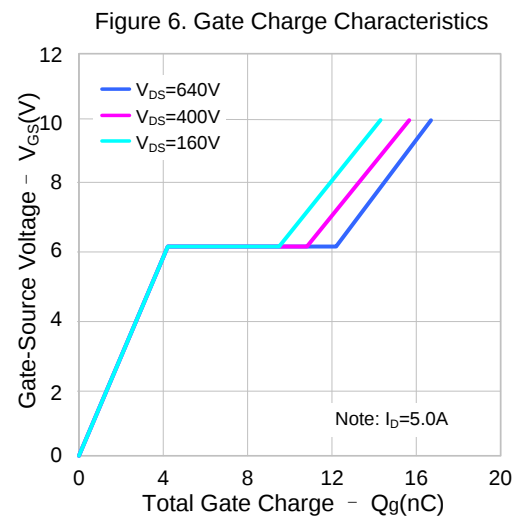
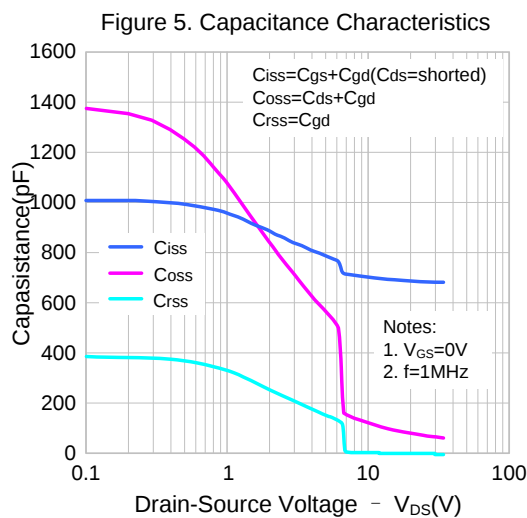
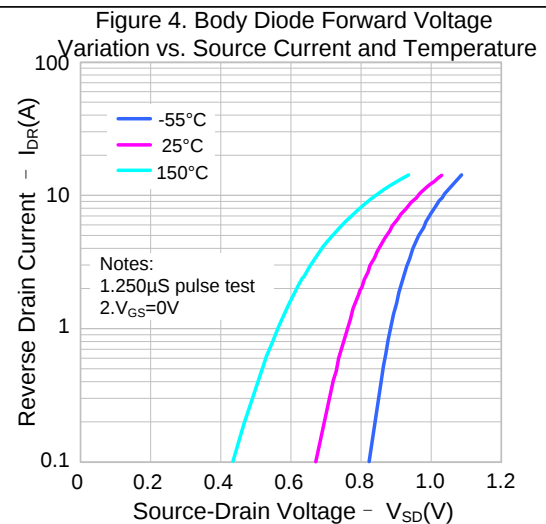
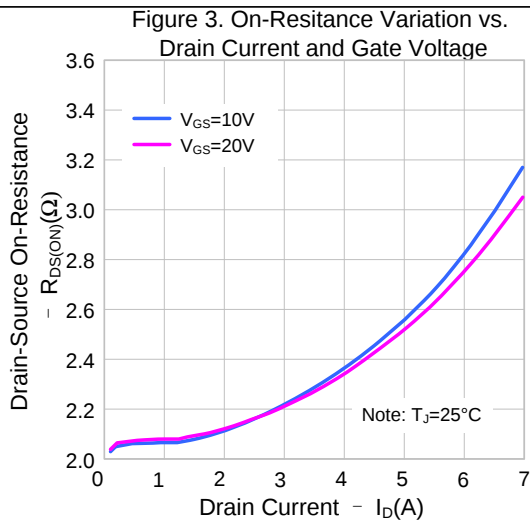
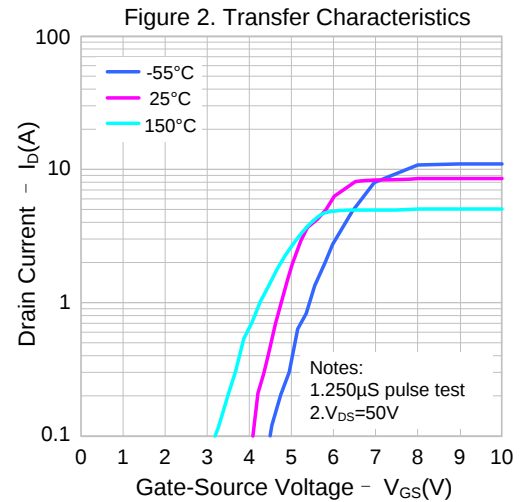
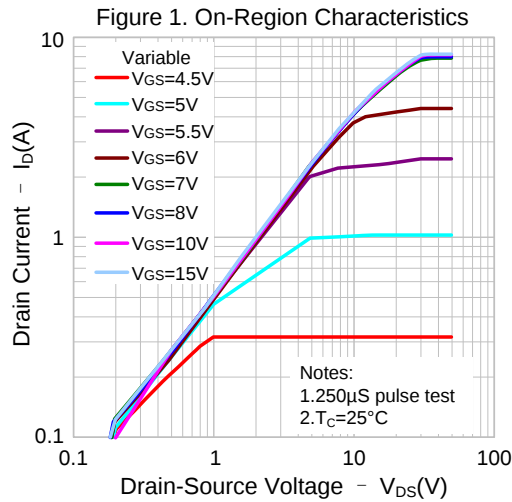
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	6.0	A
Pulsed Source Current	I _{SM}		--	--	24	
Diode Forward Voltage	V _{SD}	I _S =6.0A, V _{GS} =0V	--	--	1.4	V
Reverse Recovery Time	T _{rr}	I _S =6.0A, V _{GS} =0V, dI _F /dt=100A/μS (Note4)	--	549	--	ns
Reverse Recovery Charge	Q _{rr}		--	3.0	--	μC

Notes:

1. L=30mH, I_{AS}=4.5A, V_{DD}=60V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}≤6.0A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

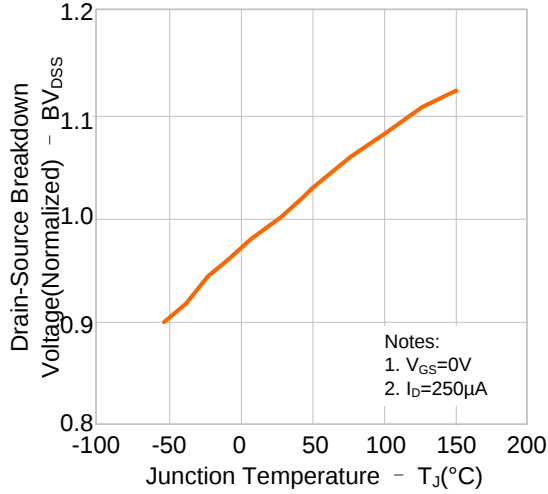


Figure 8. On-resistance Variation vs. Temperature

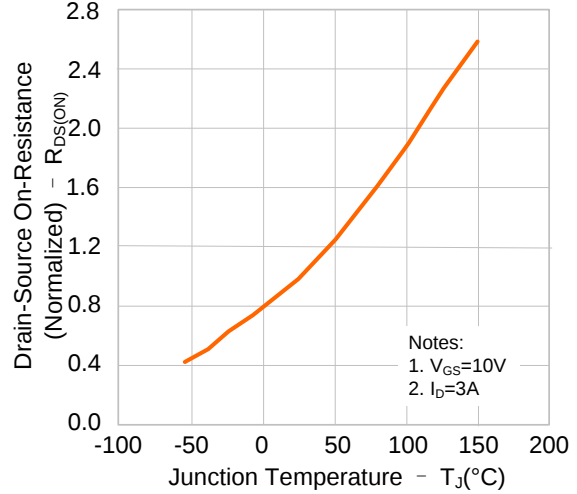


Figure 9-1. Max. Safe Operating Area(SVF6N80D/MJ)

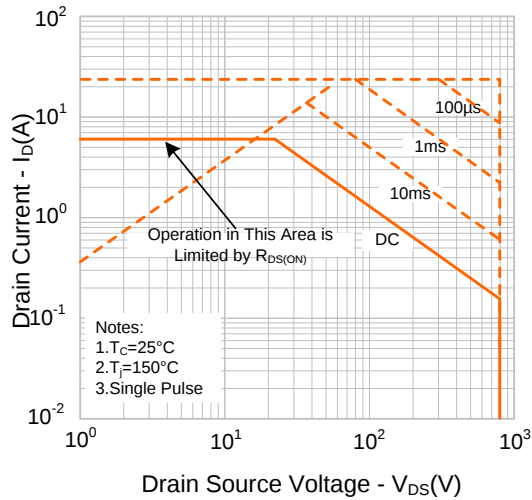


Figure 9-2. Max. Safe Operating Area(SVF6N80K)

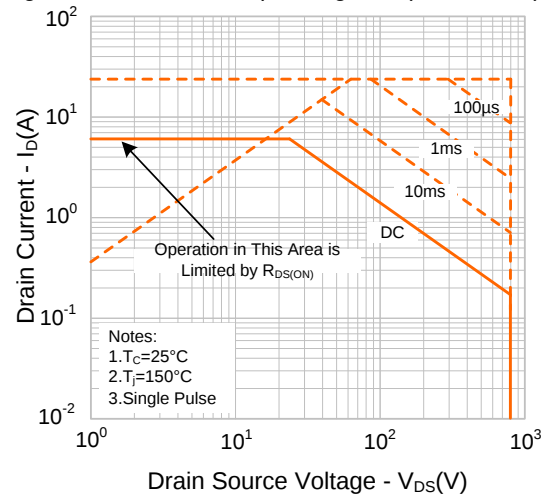
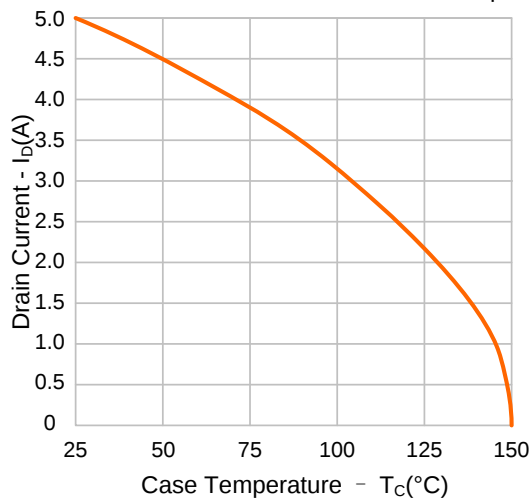
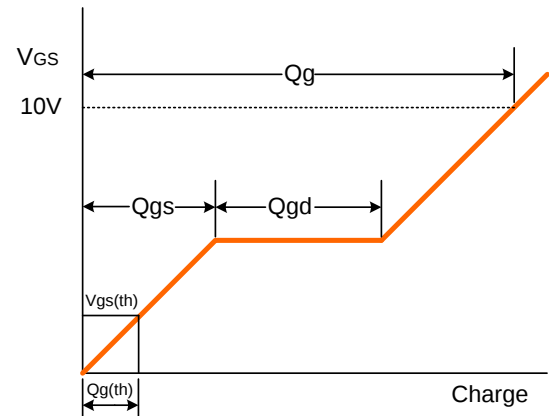
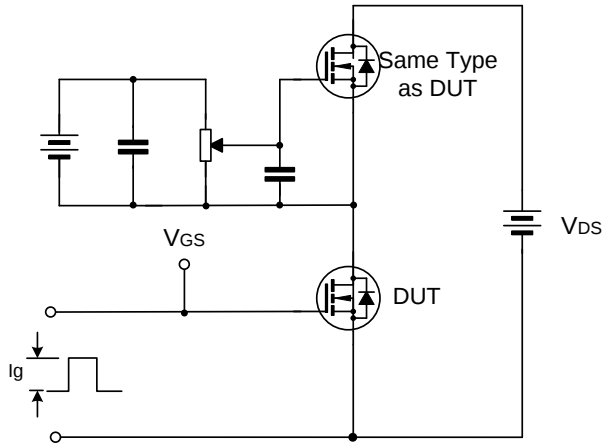


Figure 10. Maximum Drain Current vs. Case Temperature

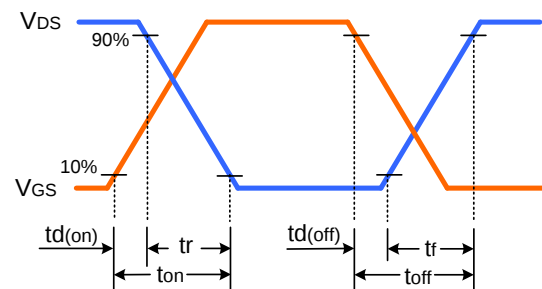
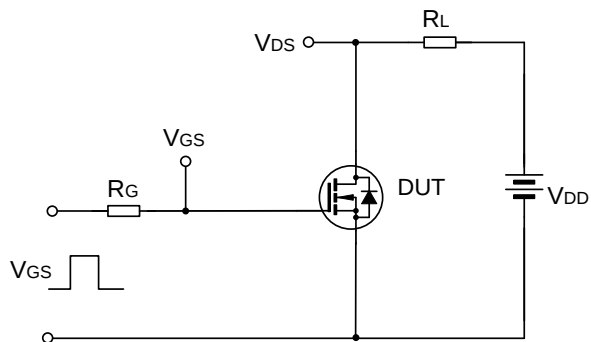


TYPICAL TEST CIRCUIT

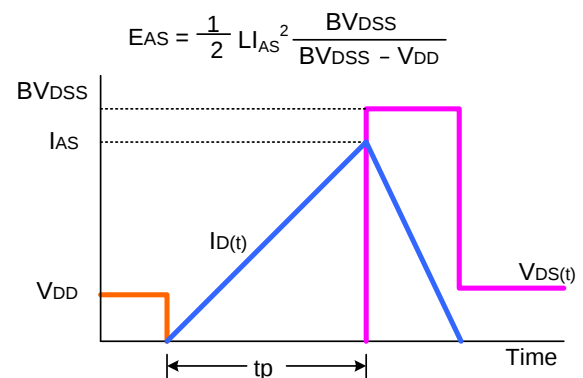
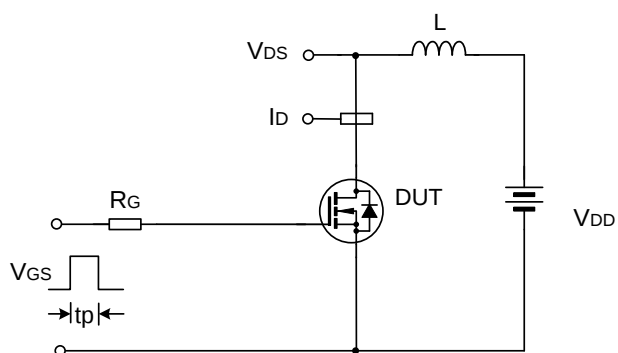
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



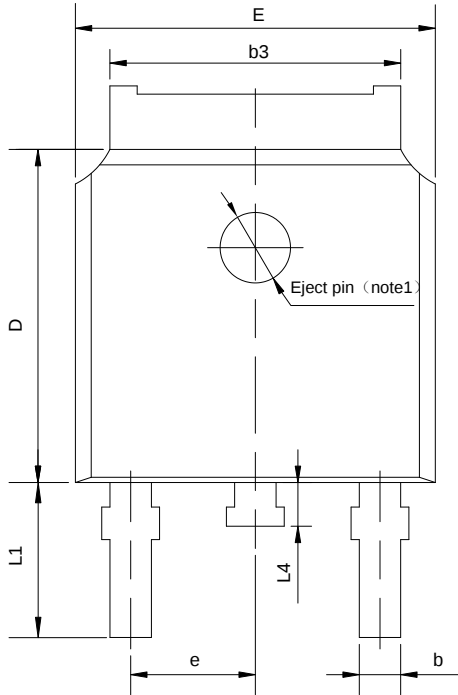
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

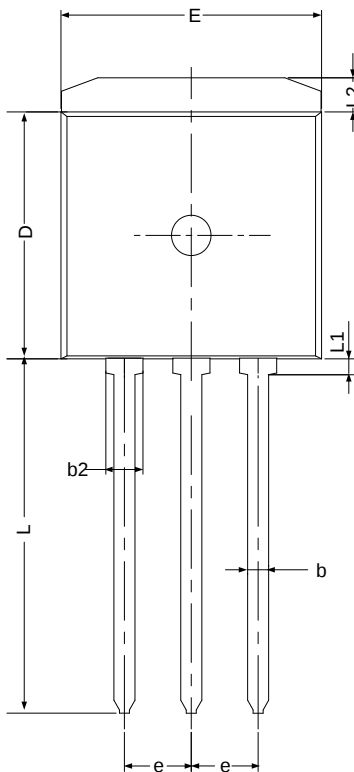
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

TO-262-3L

UNIT: mm

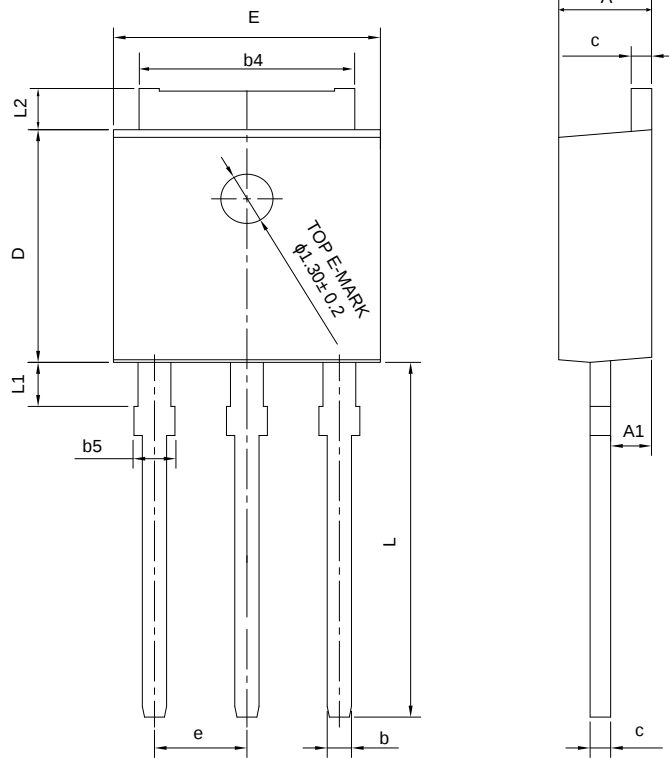


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.90
b2	1.20	—	1.50
c	0.34	—	0.65
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	—	—	0.75
L2	1.12	—	1.42

PACKAGE OUTLINE

TO-251J-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	—	0.89
b4	4.95	5.33	5.46
b5	—	—	1.05
c	0.46	—	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	—	1.50
L2	0.89	—	1.27

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Rev.: 1.3

Revision History:

1. Add SVF6N80MJ
 2. Update the template of the datasheet
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Rev.: 1.2

Revision History:

1. Add Electrical schematic and TYPICAL TEST CIRCUIT
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Rev.: 1.1

Revision History:

1. Add SVF6N80K
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Rev.: 1.0

Revision History:

1. First release
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