

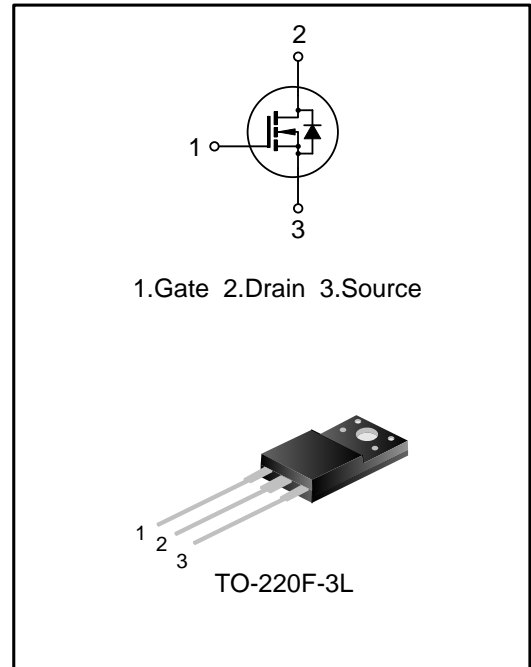
8A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF8N60F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 8A, 600V, $R_{DS(on)(typ.)}=0.96\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF8N60F	TO-220F-3L	SVF8N60F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DS}	600	V
Gate-Source Voltage		V _{GS}	±30	V
Drain Current	T _C =25°C	I _D	8.0	A
	T _C =100°C		5.0	
Drain Current Pulsed		I _{DM}	32	A
Power Dissipation(T _C =25°C)		P _D	48	W
-Derate above 25°C			0.38	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	452	mJ
Operation Junction Temperature Range		T _J	-55~+150	°C
Storage Temperature Range		T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	2.6	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =4.0A	--	0.96	1.2	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	---	770	---	pF
Output Capacitance	C _{oss}		--	99	--	
Reverse Transfer Capacitance	C _{rss}		--	9.0	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =8.0A, R _G =24Ω, V _{GS} =10V (Note 2,3)	--	15	--	ns
Turn-on Rise Time	t _r		--	34	--	
Turn-off Delay Time	t _{d(off)}		--	47	--	
Turn-off Fall Time	t _f		--	32	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =8.0A, V _{GS} =10V (Note 2,3)	--	21	--	nC
Gate-Source Charge	Q _{gs}		--	4.7	--	
Gate-Drain Charge	Q _{gd}		--	10	--	

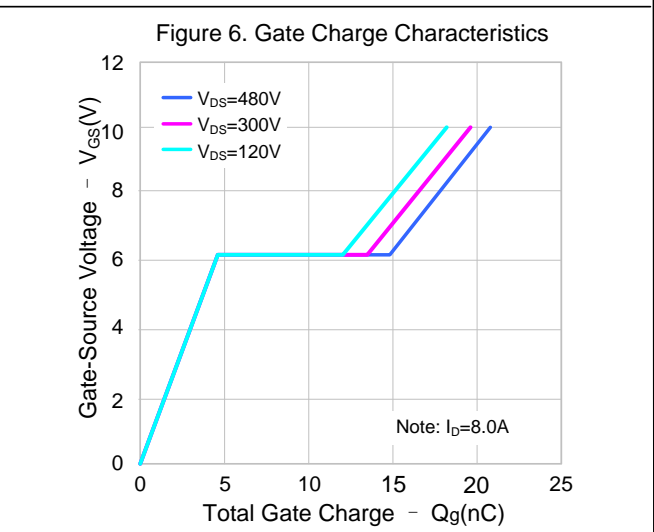
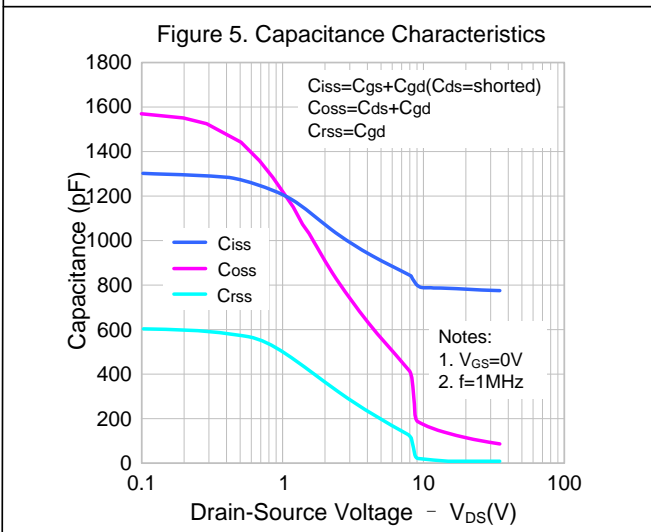
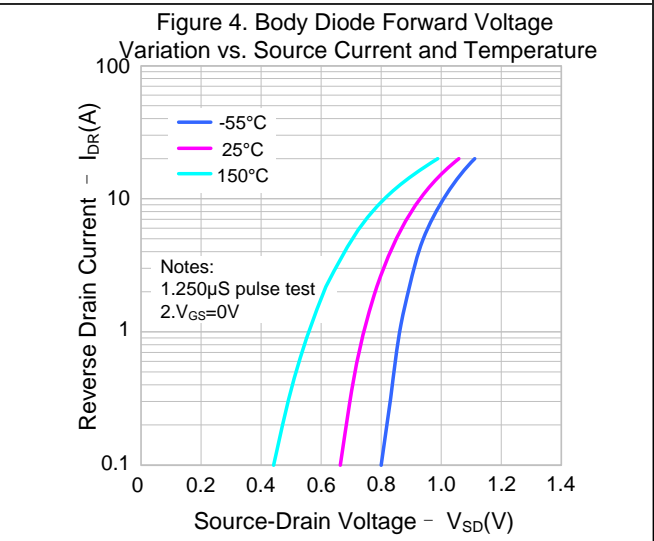
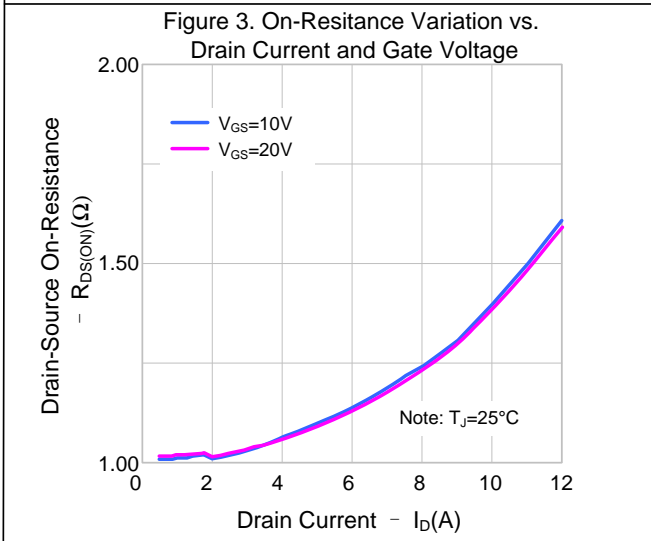
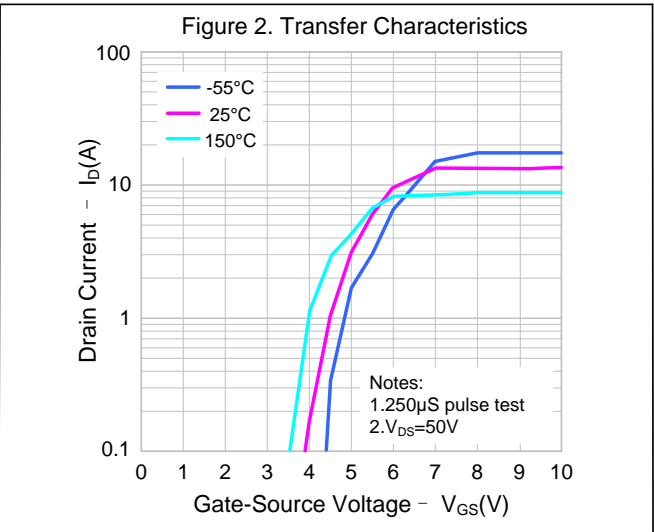
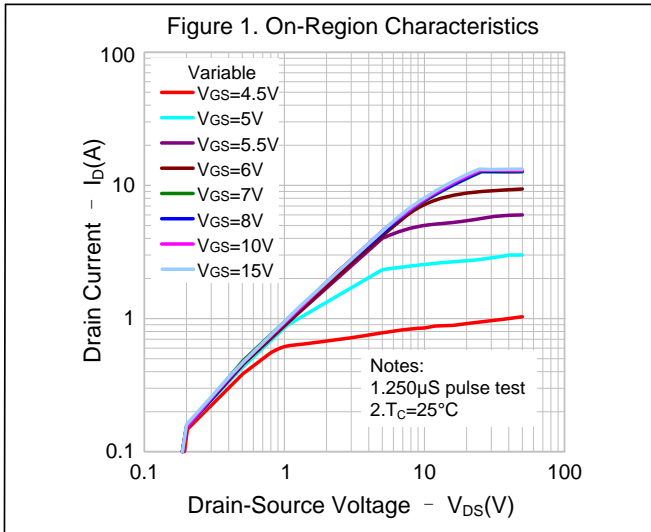
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	8.0	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	32.0	
Diode Forward Voltage	V_{SD}	$I_S=8.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=8.0A, V_{GS}=0V,$	--	510	--	ns
Reverse Recovery Charge	Q_{rr}	$di_F/dt=100A/\mu S$	--	3.4	--	μC

Notes:

1. $L=30mH, I_{AS}=5.2A, V_{DD}=100V, R_G=25\Omega,$ starting $T_{BJB}=25^\circ C;$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

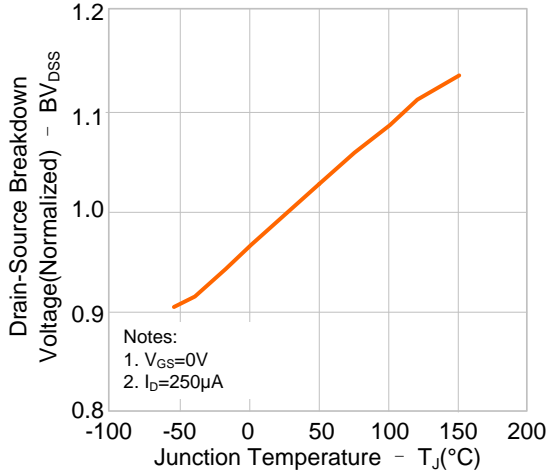


Figure 8. On-resistance Variation vs. Temperature

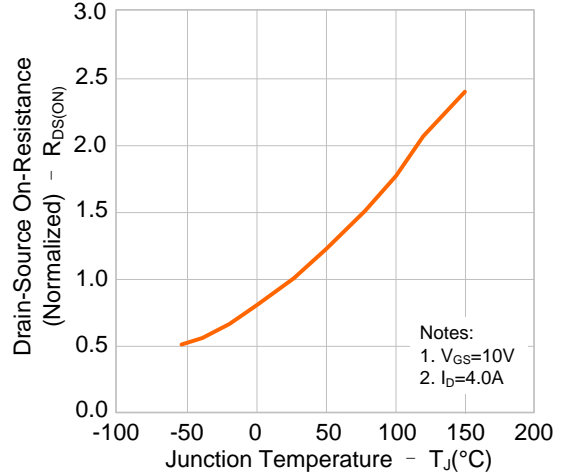


Figure 9. Max. Safe Operating Area

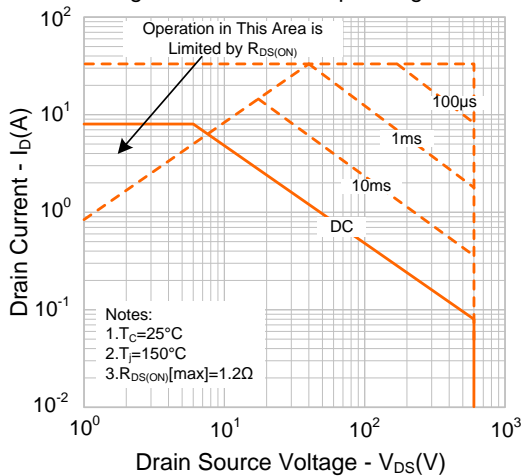
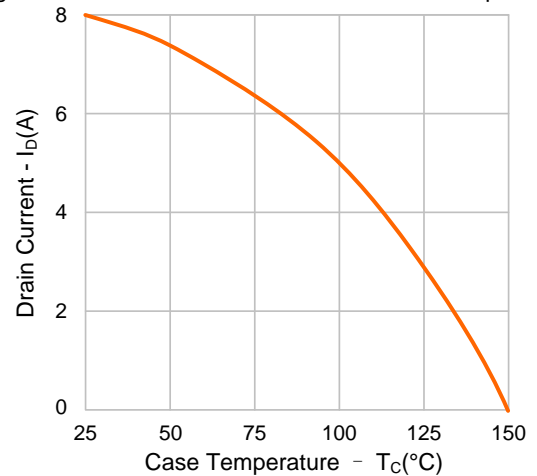
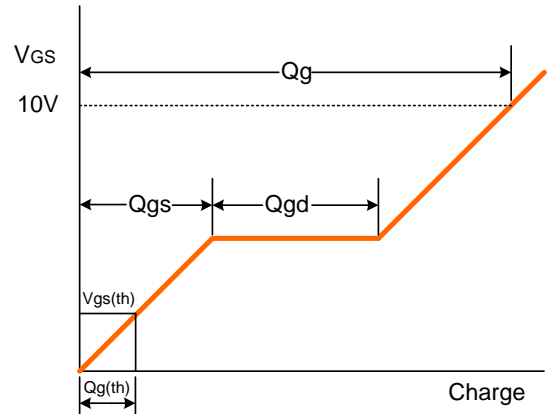
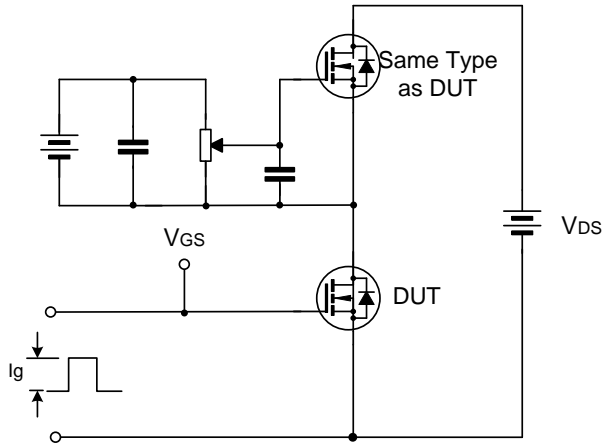


Figure 10. Maximum Drain Current vs. Case Temperature

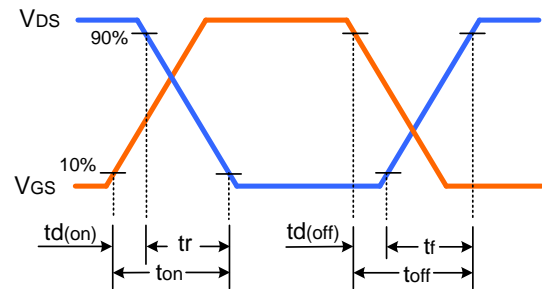
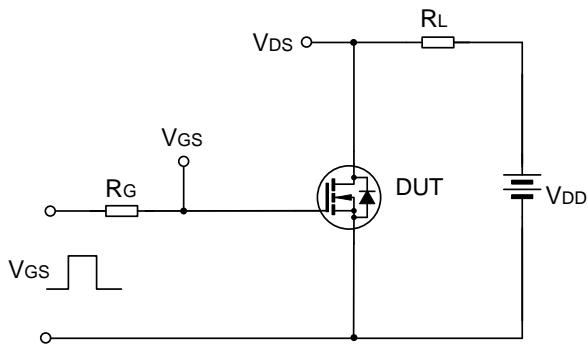


TYPICAL TEST CIRCUIT

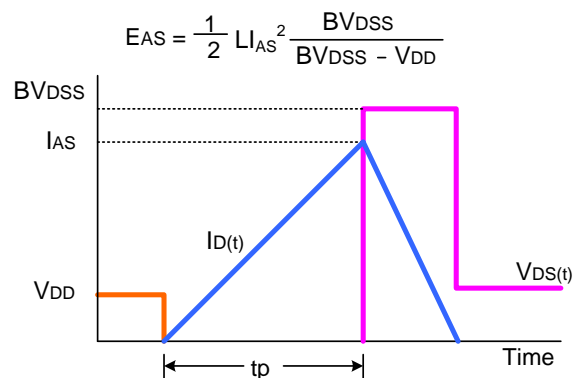
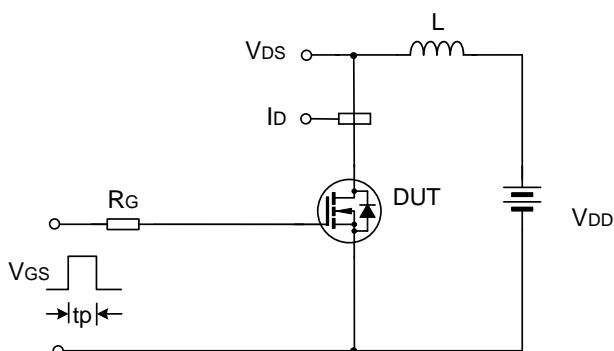
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



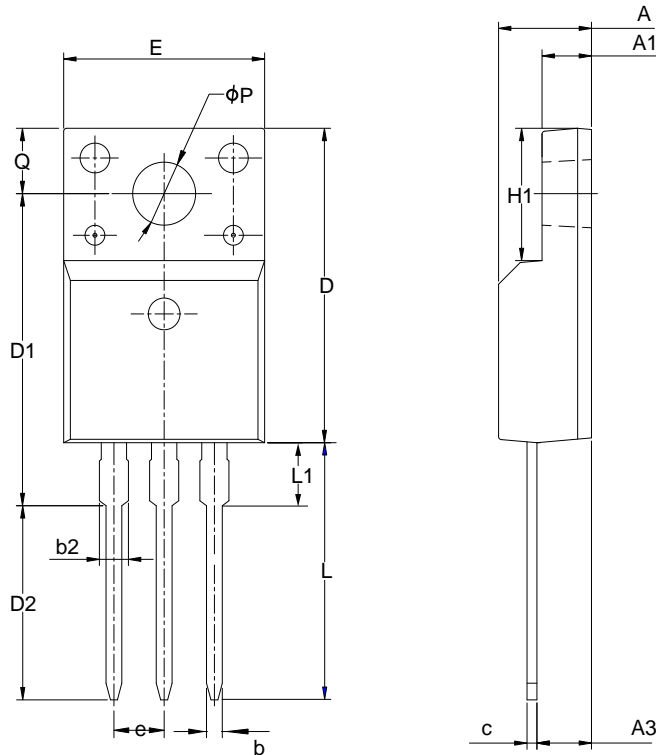
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	3.50
φP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 2.4

Revision History:

1. Update the template of the datasheet
-

Rev.: 2.3

Revision History:

1. Delete the package outline of TO-220FQ-3L
-

Rev.: 2.2

Revision History:

1. Delete the package outline of TO-220-3L
-

Rev.: 2.1

Revision History:

1. Modify Electrical characteristics
-

Rev.: 2.0

Revision History:

1. Add TO-220FQ-3L
-

Rev.: 1.9

Revision History:

1. Add $R_{DS(ON)}$ @ $T_j=125^{\circ}\text{C}$
-

Rev.: 1.8

Revision History:

1. Add R_g
 2. Modify P_D and curve
-

Rev.: 1.7

Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-220-3L
-

Rev.: 1.6

Revision History:

1. Modify the thermal characteristics
-

Rev.: 1.5

Revision History:

1. Modify the ordering information
-

Rev.: 1.4

Revision History:

1. Change the schematic diagram of MOS
-

Rev.: 1.3

Revision History:

1. Modify the typ. value of $R_{DS(on)}$
-

Rev.: 1.2

Revision History:

1. Modify the values of T_{rr} and Q_{rr}
-

Rev.: 1.1

Revision History:

1. Modify "PACKAGE OUTLINE"
-

Rev.: 1.0

Revision History:

1. Original
-