

18A, 600V N-CHANNEL MOSFET

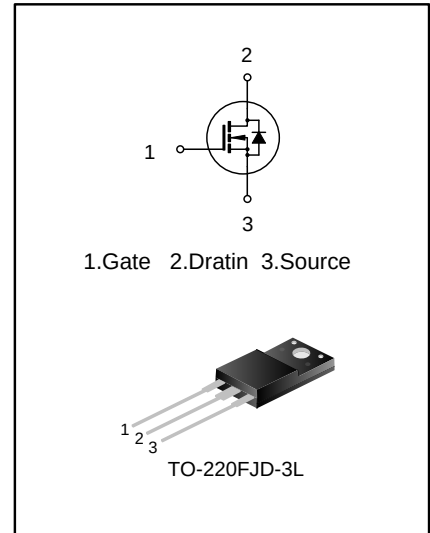
GENERAL DESCRIPTION

SVFP18N60FJD is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 18A, 600V, $R_{DS(on)}(typ.) = 0.36\Omega @ V_{GS} = 10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVFP18N60FJD	TO-220FJD-3L	P18N60FJD	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DS}	600	V
Gate-Source Voltage		V _{GS}	±30	V
Drain Current	T _C =25°C	I _D	18	A
	T _C =100°C		11	
Drain Current Pulsed		I _{DM}	72	A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	54	W
			0.43	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	1185	mJ
Reverse Diode dv/dt (Note 2)		dv/dt	4.5	V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T _J	-55~+150	°C
Storage Temperature Range		T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	2.31	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =9.0A	--	0.36	0.45	Ω
Gate Resistance	R _g	f=1.0MHz	--	5.0	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	2395	--	pF
Output Capacitance	C _{oss}		--	250	--	
Reverse Transfer Capacitance	C _{rss}		--	7.9	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =18A, R _G =25Ω, (Note4,5)	--	39	--	ns
Turn-on Rise Time	t _r		--	60	--	
Turn-off Delay Time	t _{d(off)}		--	128	--	
Turn-off Fall Time	t _f		--	56	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =18A, V _{GS} =10V, (Note4,5)	--	46	--	nC
Gate-Source Charge	Q _{gs}		--	17	--	
Gate-Drain Charge	Q _{gd}		--	15	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	18	A
Pulsed Source Current	I_{SM}		--	--	72	
Diode Forward Voltage	V_{SD}	$I_S=18\text{ A}, V_{GS}=0\text{ V}$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=18\text{ A}, V_{GS}=0\text{ V},$ $di_F/dt=100\text{ A}/\mu\text{s}$ (Note 4)	--	616	--	ns
Reverse Recovery Charge	Q_{rr}		--	7.40	--	μC

Notes:

1. $L=30\text{ mH}$, $I_{AS}=8.25\text{ A}$, $V_{DD}=50\text{ V}$, $R_G=25\Omega$, starting temperature $T_J=25^\circ\text{C}$;
2. $V_{DS}=0\sim 400\text{ V}$, $I_{SD}\leq 18\text{ A}$, $T_J=25^\circ\text{C}$;
3. $V_{DS}=0\sim 480\text{ V}$;
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

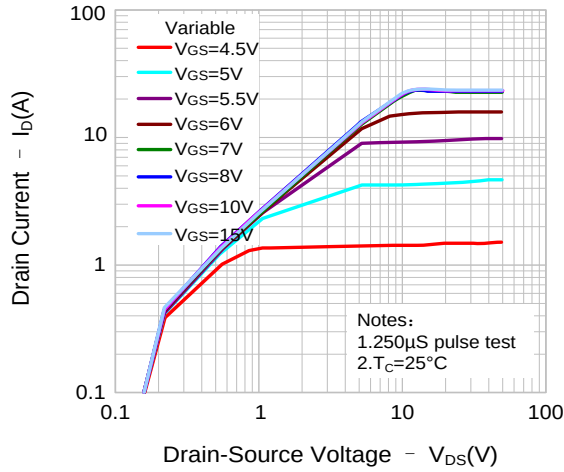


Figure 2. Transfer Characteristics

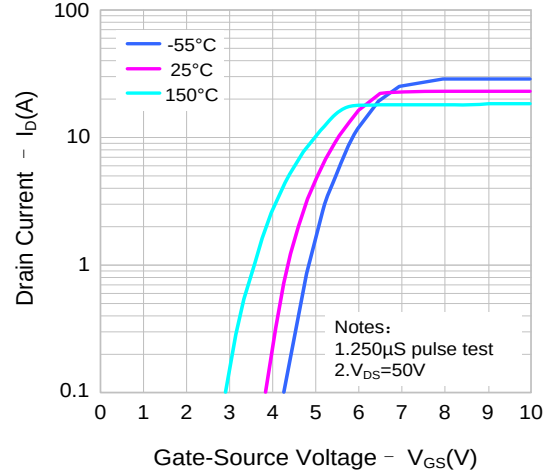


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

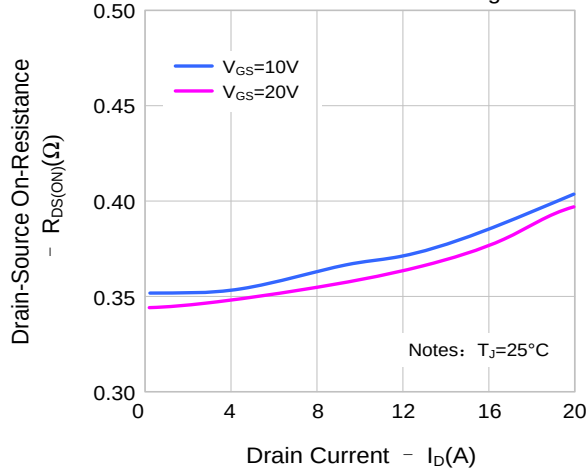


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

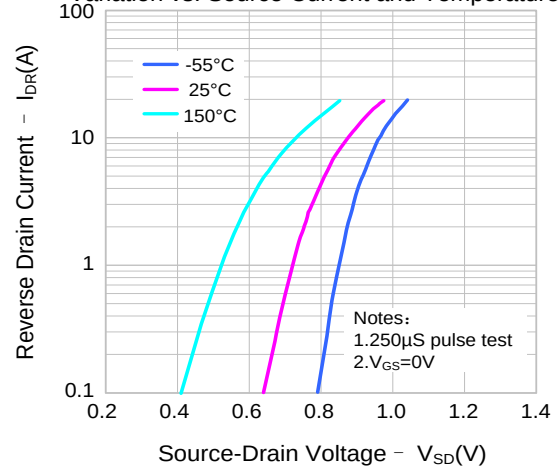


Figure 5. Capacitance Characteristics

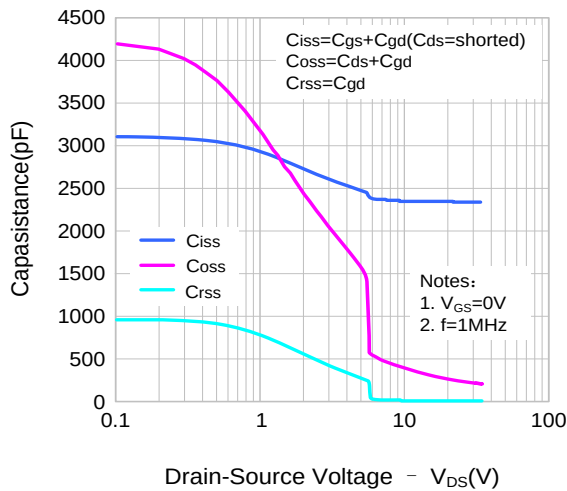
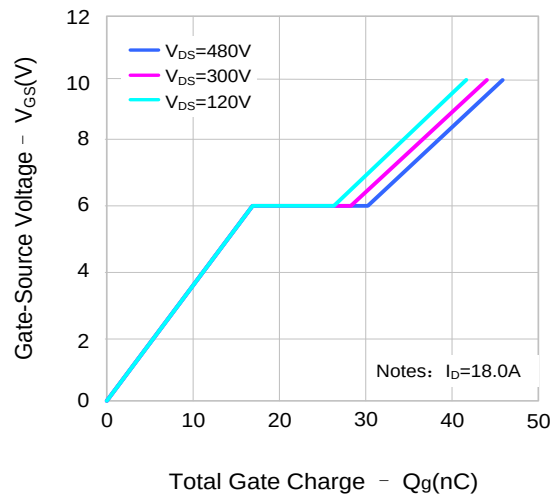


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

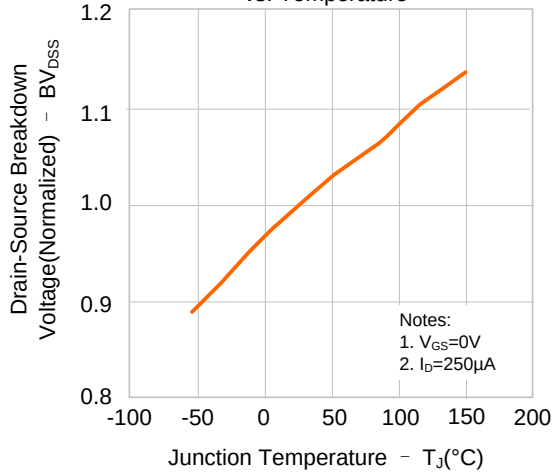


Figure 8. On-resistance Variation vs. Temperature

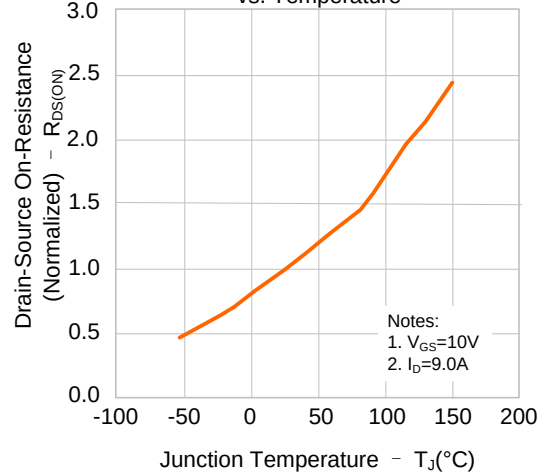


Figure 9. Max. Safe Operating Area

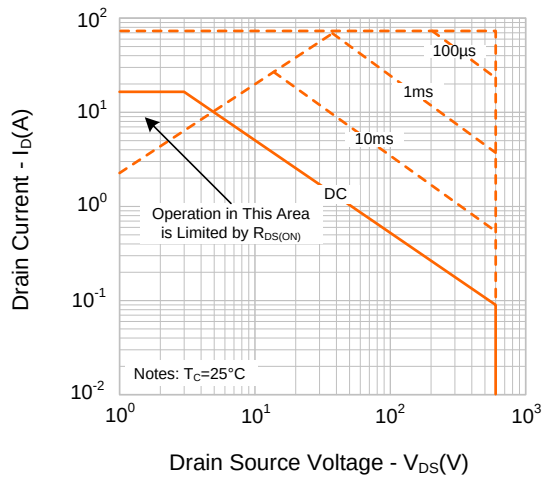
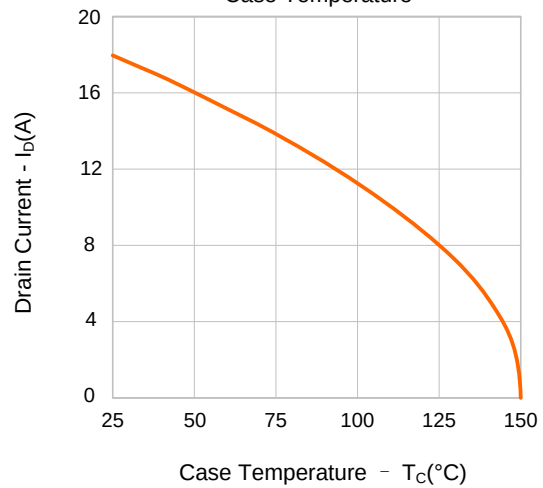
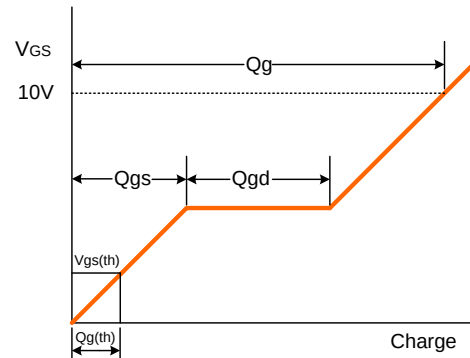
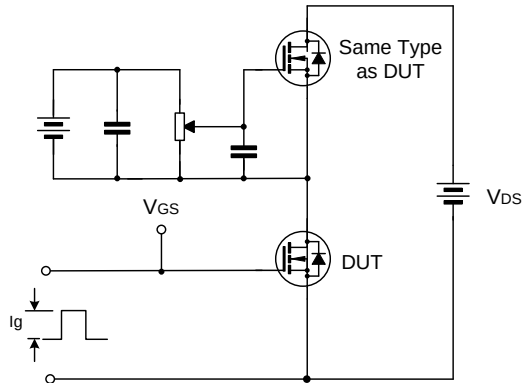


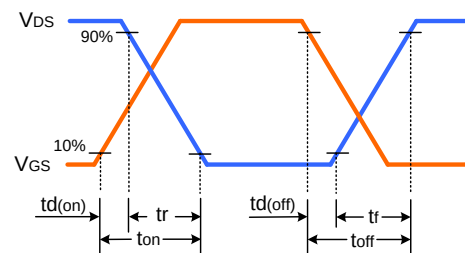
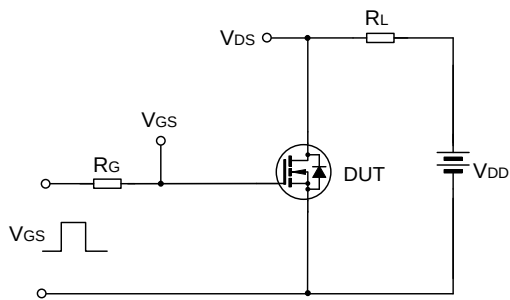
Figure 10. Maximum Drain Current vs. Case Temperature



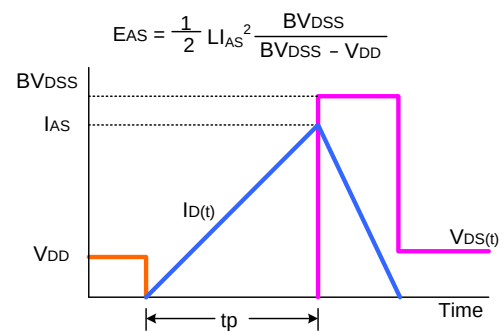
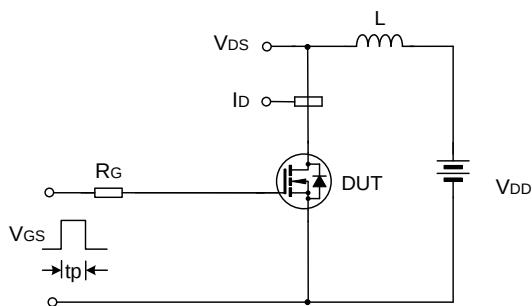
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

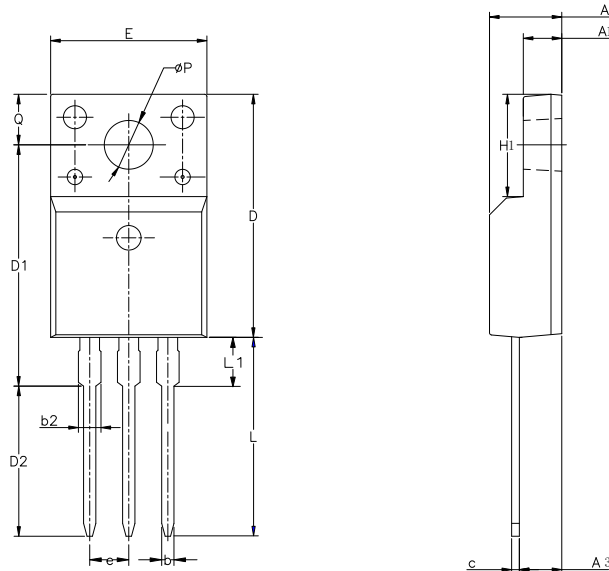


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220FJD-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 1.1

Revision History:

1. Modify Electrical schematic and TYPICAL TEST CIRCUIT
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Rev.: 1.0

Revision History:

1. First release
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