

5A, 650V N-CHANNEL MOSFET

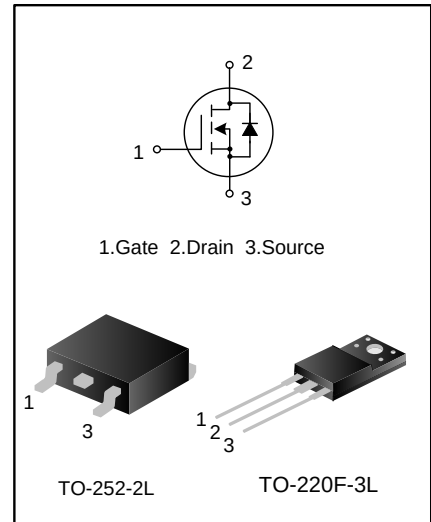
GENERAL DESCRIPTION

The SVF5N65D/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 5A, 650V, $R_{DS(on)(typ.)}=2.1\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF5N65DTR	TO-252-2L	SVF5N65D	Halogen free	Tape&Reel
SVF5N65F	TO-220F-3L	SVF5N65F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVF5N65D	SVF5N65F	
Drain-Source Voltage		V _{DS}	650		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	5.0		A
	T _C =100°C		3.1		
Drain Current Pulsed		I _{DM}	20		A
Power Dissipation(T _C =25°C) - Derate above 25°C		P _D	79	30	W
			0.53	0.24	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	242		mJ
Operation Junction Temperature Rating		T _J	-55~+150		°C
Storage Temperature Rating		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF5N65D	SVF5N65F	
Thermal Resistance, Junction-to-Case	R _{θJC}	1.90	4.17	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V	--	--	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.5A	--	2.1	2.5	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	--	471	--	pF
Output Capacitance	C _{oss}		--	58	--	
Reverse Transfer Capacitance	C _{rss}		--	5.5	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =325V, I _D =5.0A, R _G =24Ω (Note 2,3)	--	13.87	--	ns
Turn-on Rise Time	t _r		--	31.93	--	
Turn-off Delay Time	t _{d(off)}		--	43.53	--	
Turn-off Fall Time	t _f		--	33.73	--	
Total Gate Charge	Q _g	V _{DS} =520V, I _D =5.0A, V _{GS} =10V (Note 2,3)	--	13.63	--	nC
Gate-Source Charge	Q _{gs}		--	2.96	--	
Gate-Drain Charge	Q _{gd}		--	6.86	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5	A
Pulsed Source Current	I_{SM}		--	--	20	
Diode Forward Voltage	V_{SD}	$I_S=5.0A$, $V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=5.0A$, $V_{GS}=0V$, $dI_F/dt=100A/\mu s$	--	476	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.3	--	μC

Notes:

1. $L=30mH$, $I_{AS}=3.78A$, $V_{DD}=100V$, $R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

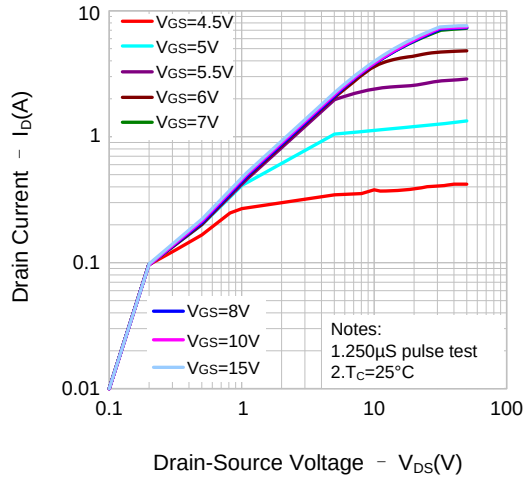


Figure 2. Transfer Characteristics

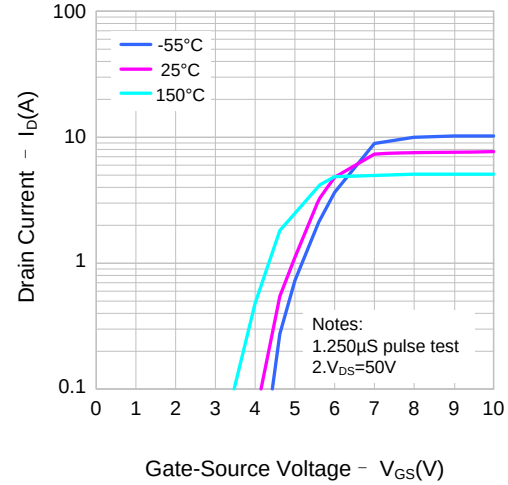


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

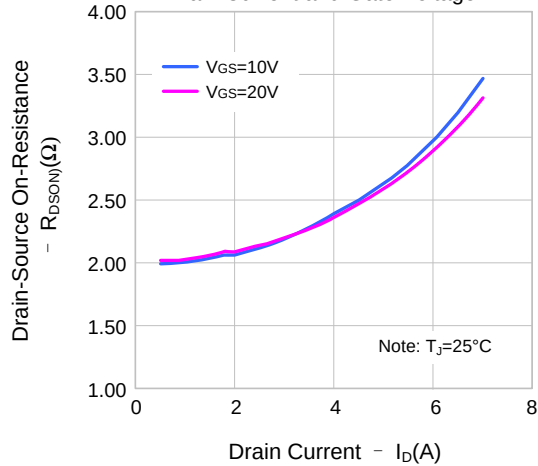


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

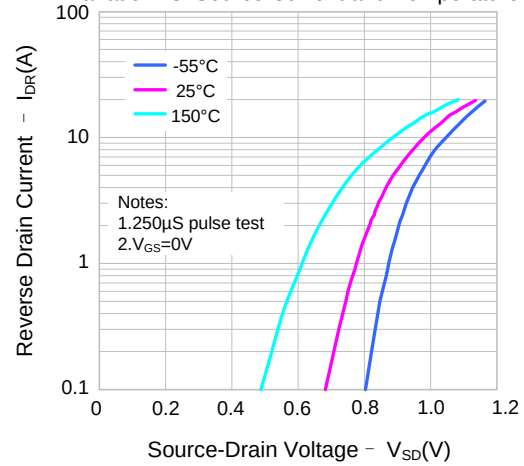


Figure 5. Capacitance Characteristics

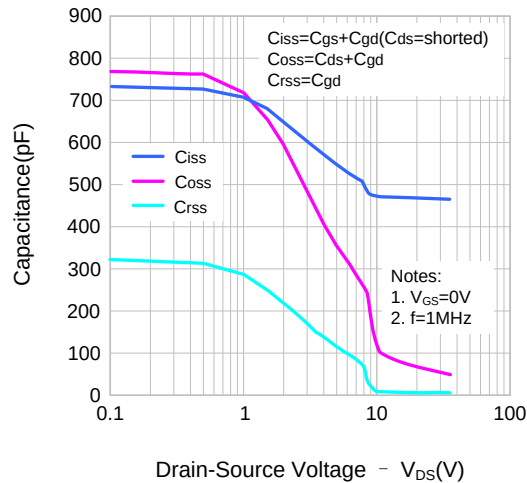
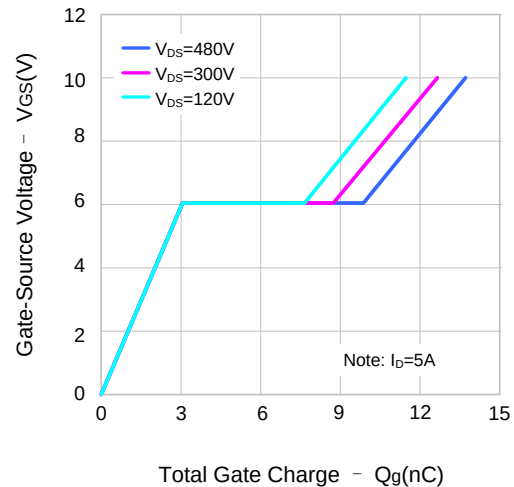


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

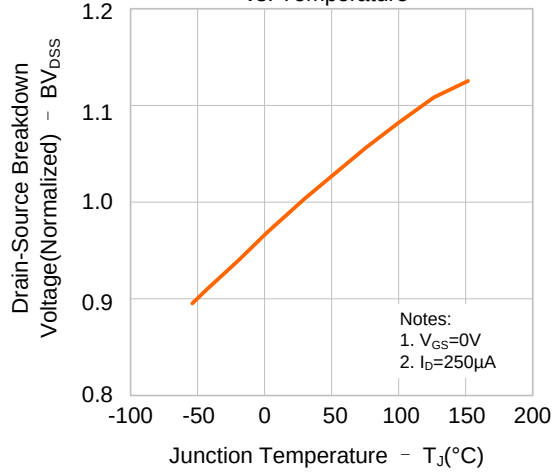


Figure 8. On-resistance Variation vs. Temperature

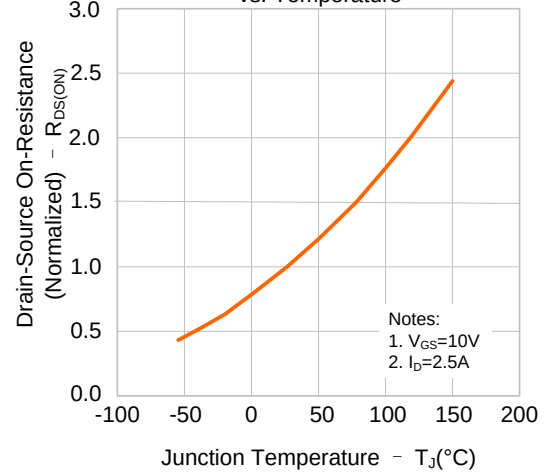


Figure 9-1. Max. Safe Operating Area (SVF5N65D)

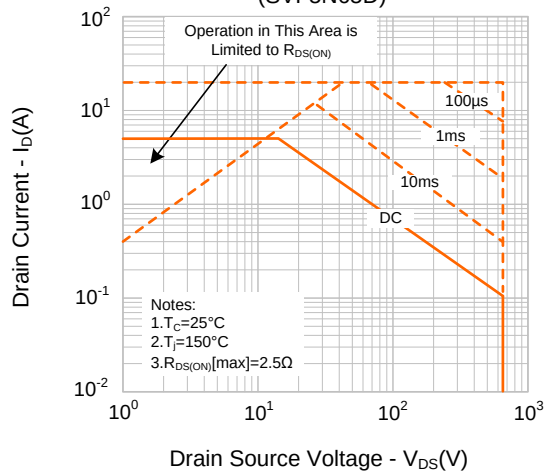


Figure 9-2. Max. Safe Operating Area (SVF5N65F)

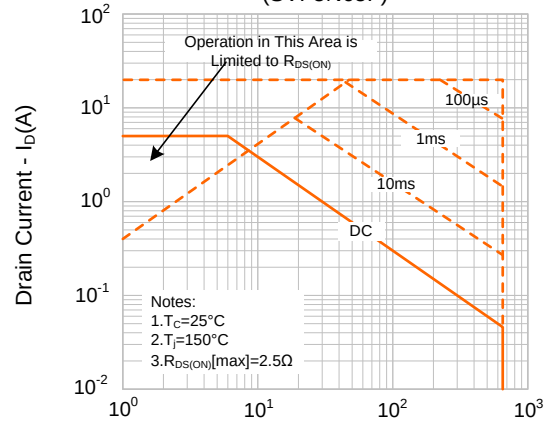
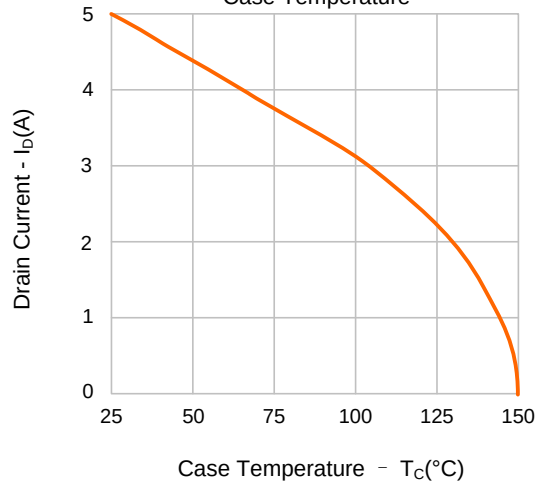
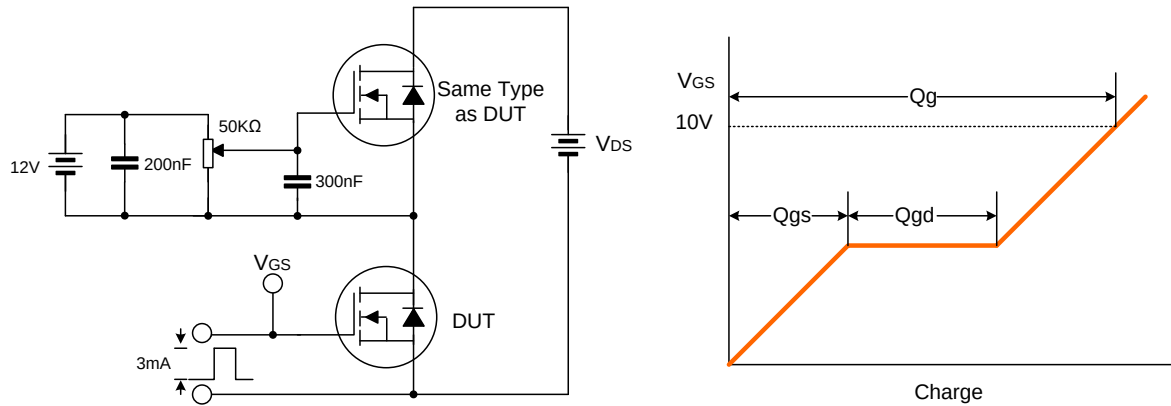


Figure 10. Maximum Drain Current vs. Case Temperature

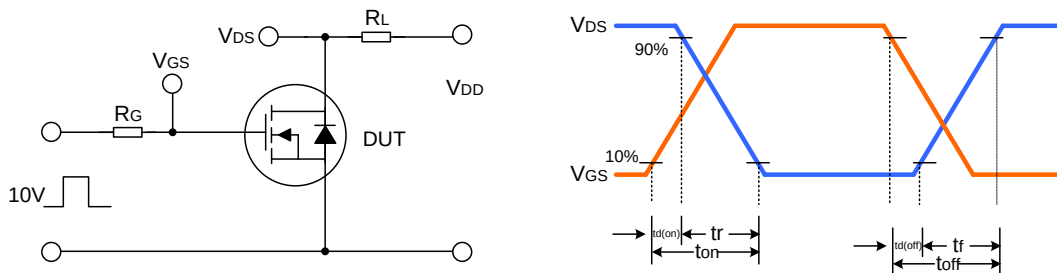


TYPICAL TEST CIRCUIT

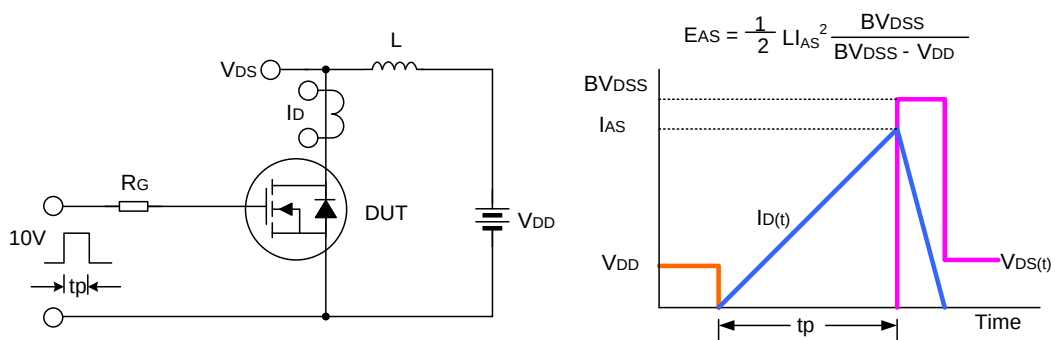
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



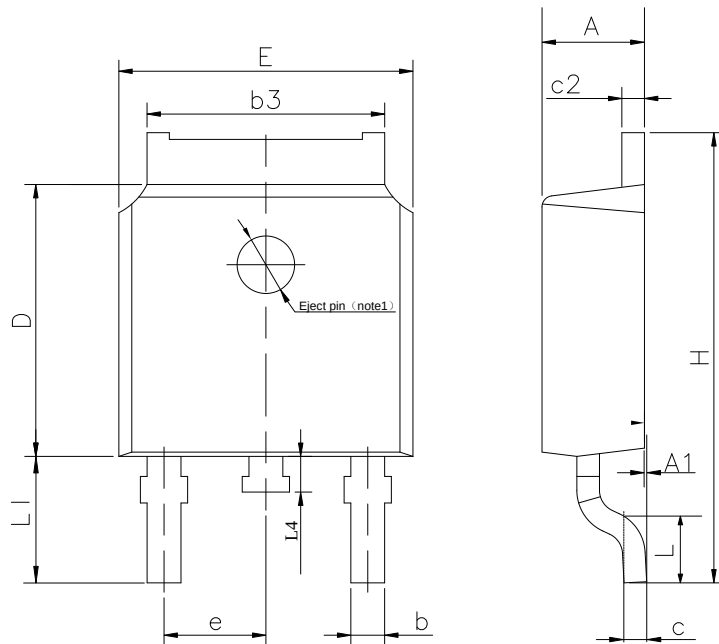
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

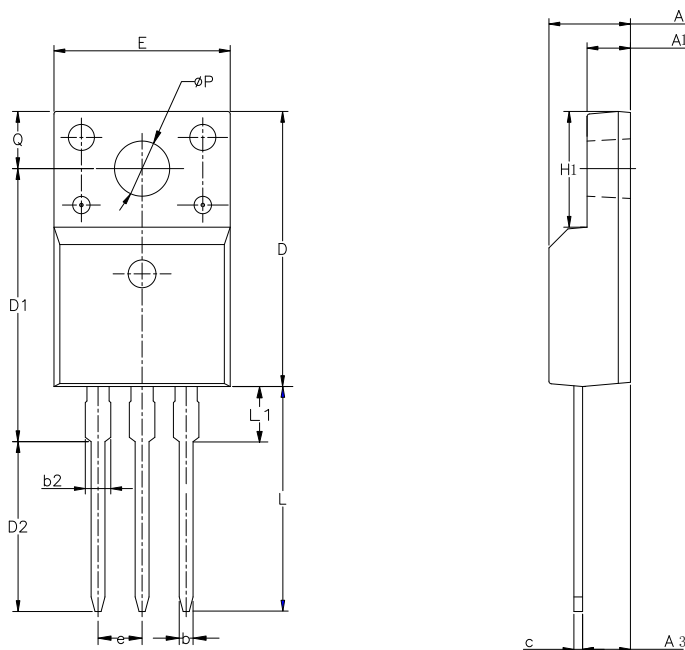


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-220F-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Part No.: **SVF5N65D/F**Document Type: **Datasheet**Copyright: **HANGZHOU SILAN MICROELECTRONICS CO.,LTD**Website: **<http://www.silan.com.cn>**Rev.: **1.1**

Revision History:

1. Add TO-220F-3L

Rev.: **1.0**

Revision History:

1. First release