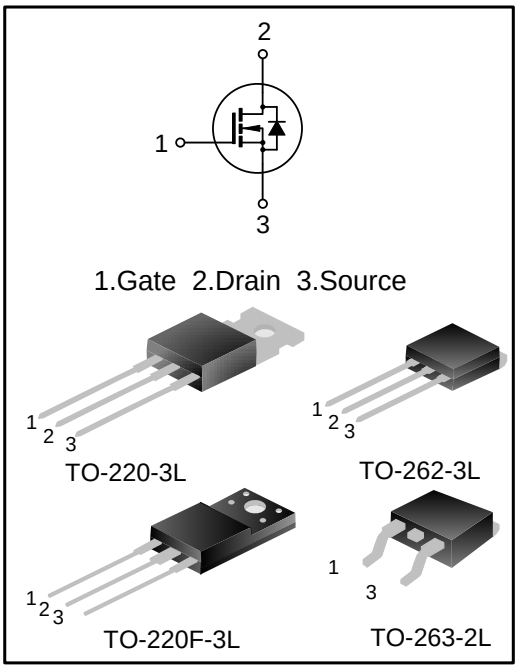
10A, 650V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF10N65T/F/K/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 10A,650V,$R_{DS(on)(typ.)}$=0.80Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF10N65T	TO-220-3L	SVF10N65T	Pb free	Tube
SVF10N65F	TO-220F-3L	SVF10N65F	Pb free	Tube
SVF10N65K	TO-262-3L	SVF10N65K	Pb free	Tube
SVF10N65S	TO-263-2L	SVF10N65S	Halogen free	Tube
SVF10N65STR	TO-263-2L	SVF10N65S	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings				Unit
			SVF10N 65F	SVF10N 65T	SVF10N 65K	SVF10N 65S	
Drain-Source Voltage		V_{DS}	650				V
Gate-Source Voltage		V_{GS}	±30				V
Drain Current	T_C=25°C	I_D	10				A
	T_C=100°C		6.3				
Drain Current Pulsed		I_{DM}	40				A
Power Dissipation(T_C=25°C)		P_D	50	156	150	150	W
-Derate above 25°C			0.4	1.25	1.20	1.20	W/°C
Single Pulsed Avalanche Energy (Note1)		E_{AS}	618				mJ
Operation Junction Temperature Range		T_J	-55～+150				°C
Storage Temperature Range		T_{stg}	-55～+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SVF10N 65F	SVF10N 65K	SVF10N 65T	SVF10N 65S	
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	2.5	0.83	0.8	0.83	°C/W
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_j=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS},I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=5.0A	--	0.8	1.0	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	1100	--	pF
Output Capacitance	C_{oss}		--	130	--	
Reverse Transfer Capacitance	C_{rss}		--	13	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V,I_D=10A, R_G=25Ω (Note 2,3)	--	21	--	ns
Turn-on Rise Time	t_r		--	41	--	
Turn-off Delay Time	$t_{d(off)}$		--	82	--	
Turn-off Fall Time	t_f		--	43	--	
Total Gate Charge	Q_g	V_{DS}=520V,I_D=10A, V_{GS}=10V (Note 2,3)	--	29	--	nC
Gate-Source Charge	Q_{gs}		--	6.2	--	
Gate-Drain Charge	Q_{gd}		--	13	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction	--	--	10	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	40	
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=10A,V_{GS}=0V,	--	561	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μS (Note:2)	--	4.3	--	μC

Notes:

1. L=30mH,I_{AS}=6.0A,V_{DD}=100V,R_G=25Ω, starting T_J=25°C;
2. Pulse Test:Pulse width≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

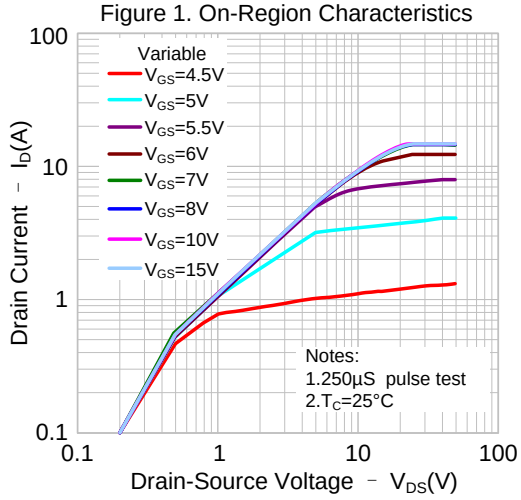


Figure 2. Transfer Characteristics

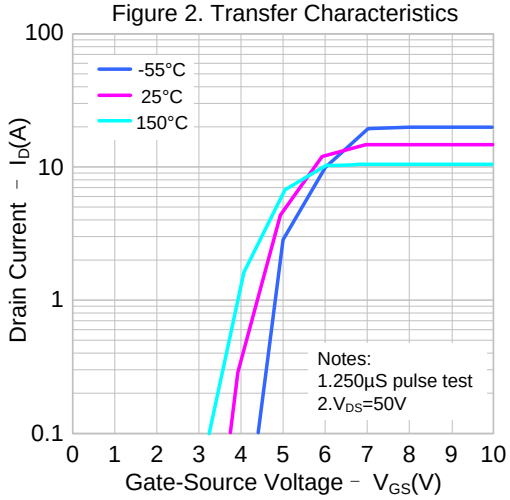


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

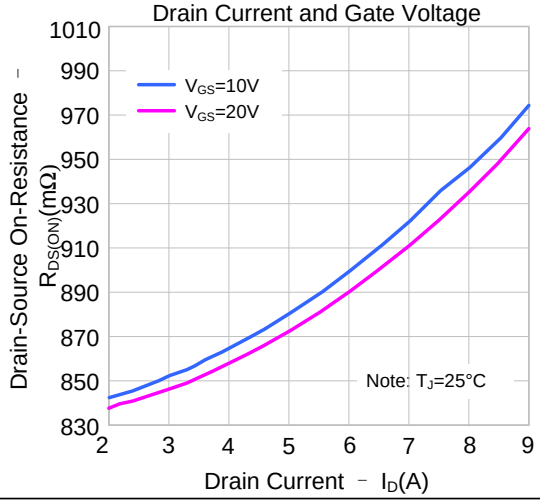


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

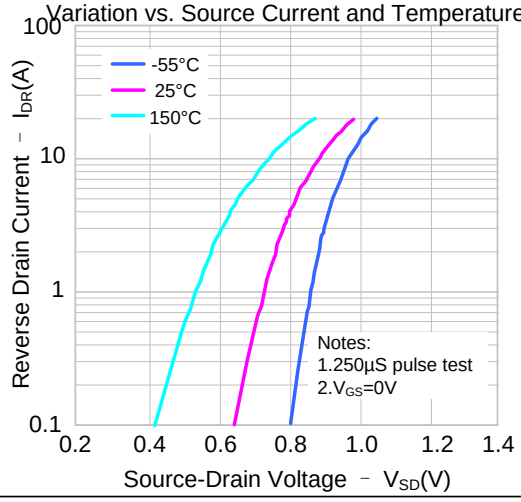


Figure 5. Capacitance Characteristics

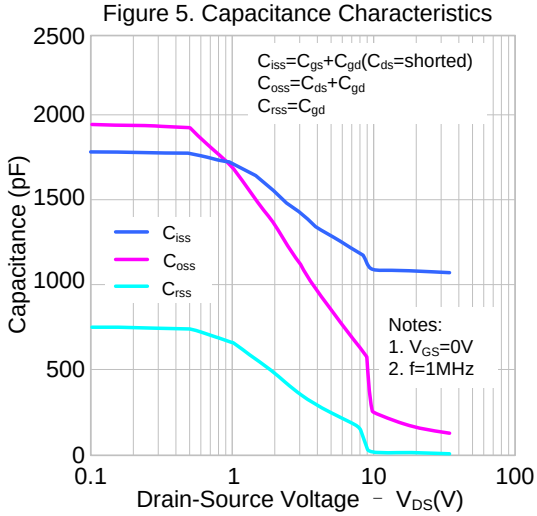
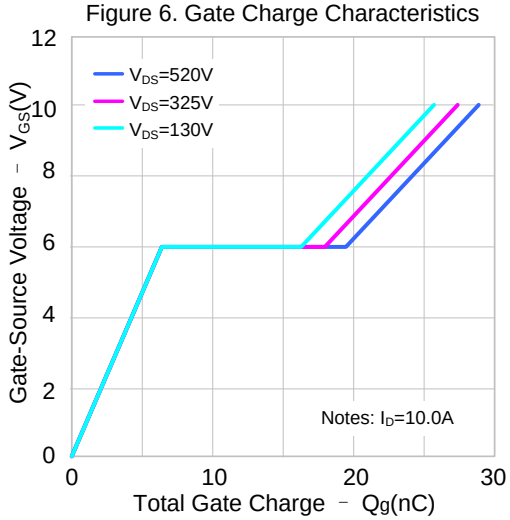


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

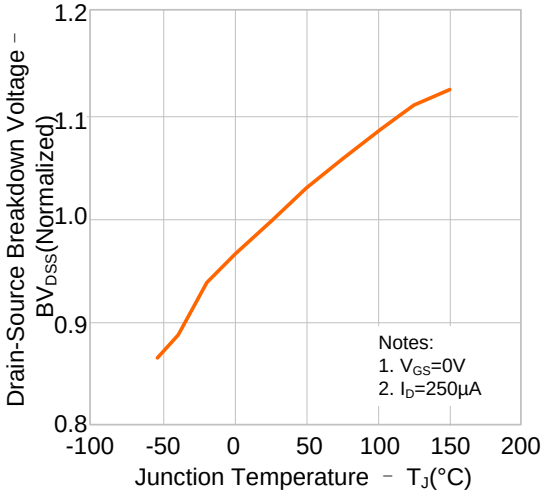


Figure 8. On-resistance vs. Temperature

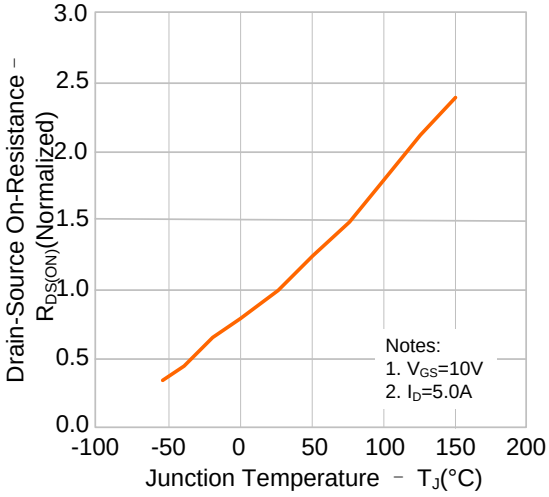


Figure 9-1. Max. Safe Operating Area(SVF10N65F)

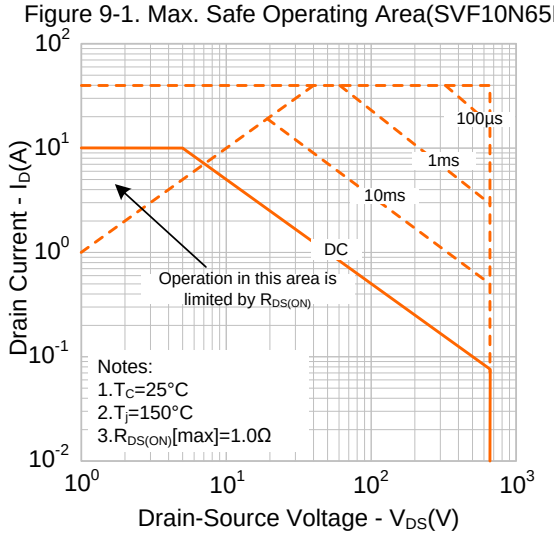


Figure 9-2. Max. Safe Operating Area(SVF10N65K)

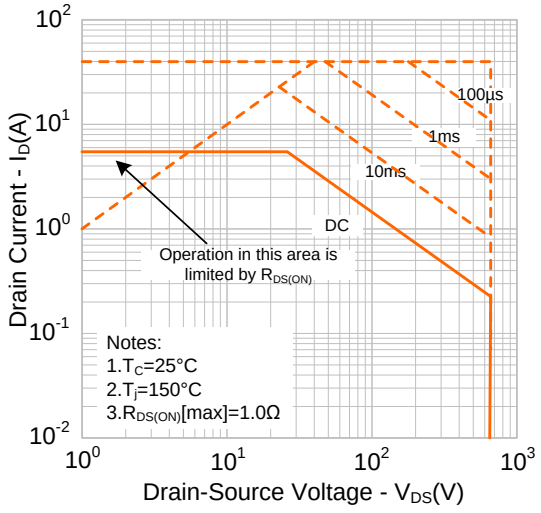


Figure 9-3. Max. Safe Operating Area(SVF10N65T)

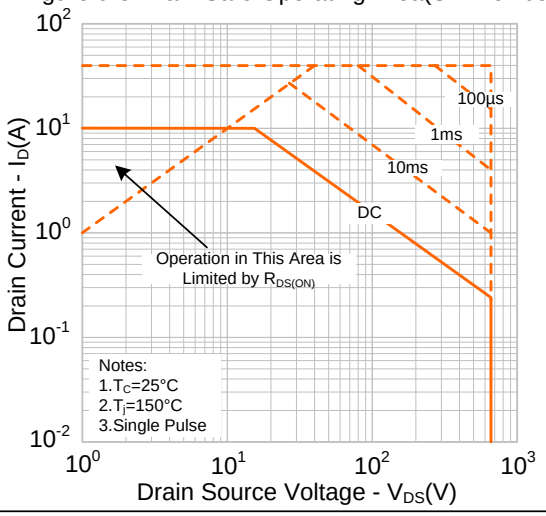
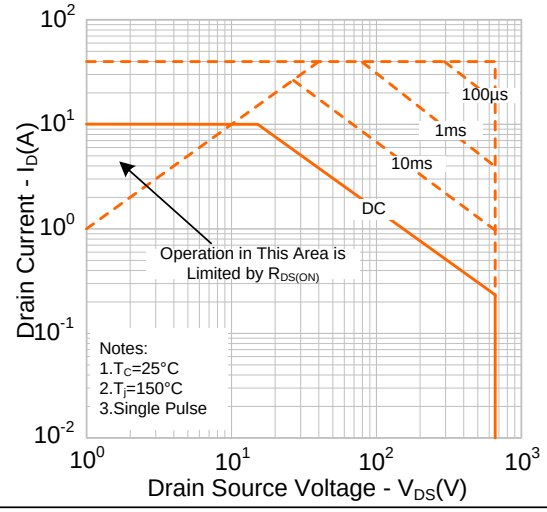
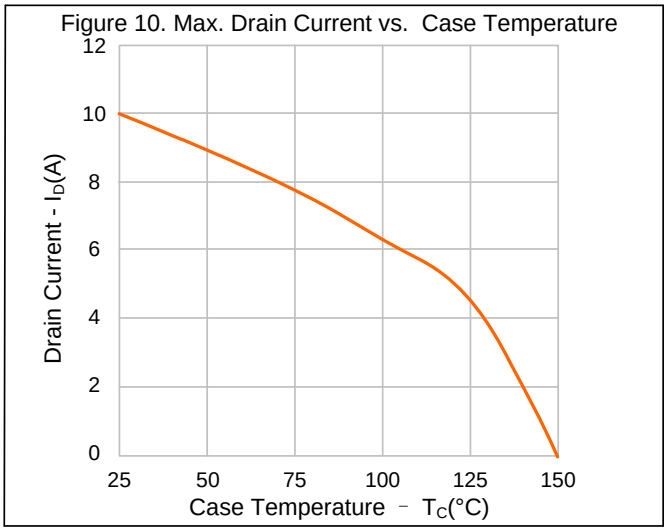


Figure 9-4. Max. Safe Operating Area(SVF10N65S)



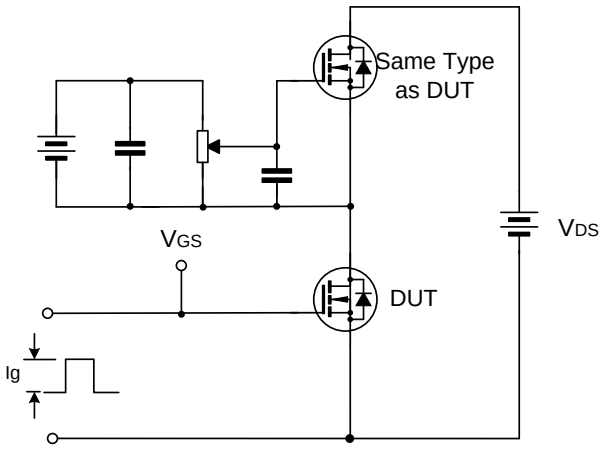
TYPICAL CHARACTERISTICS (CONTINUED)

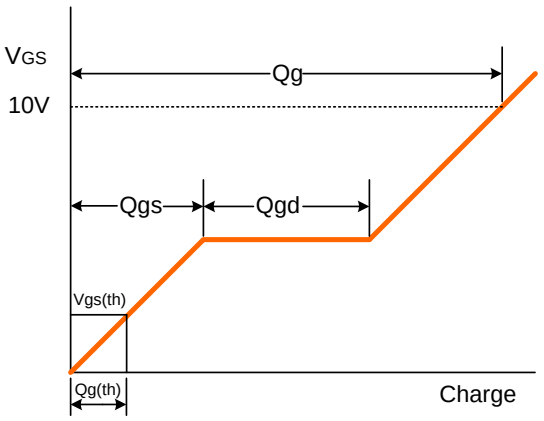
Figure 10. Max. Drain Current vs. Case Temperature



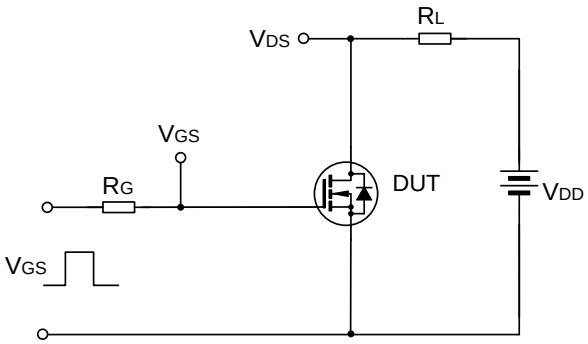
TYPICAL TEST CIRCUIT

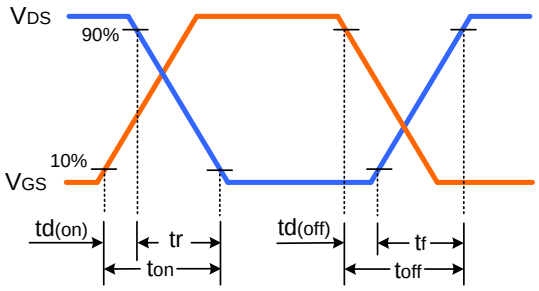
Gate Charge Test Circuit & Waveform



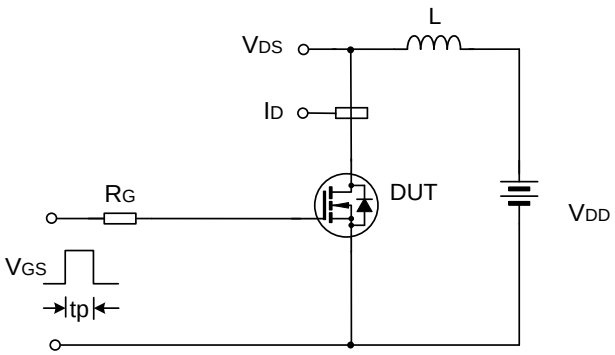


Resistive Switching Test Circuit & Waveform

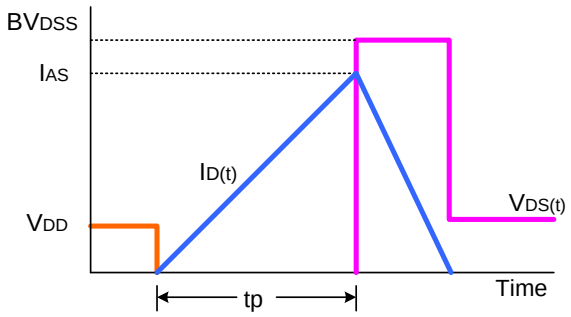




Unclamped Inductive Switching Test Circuit & Waveform



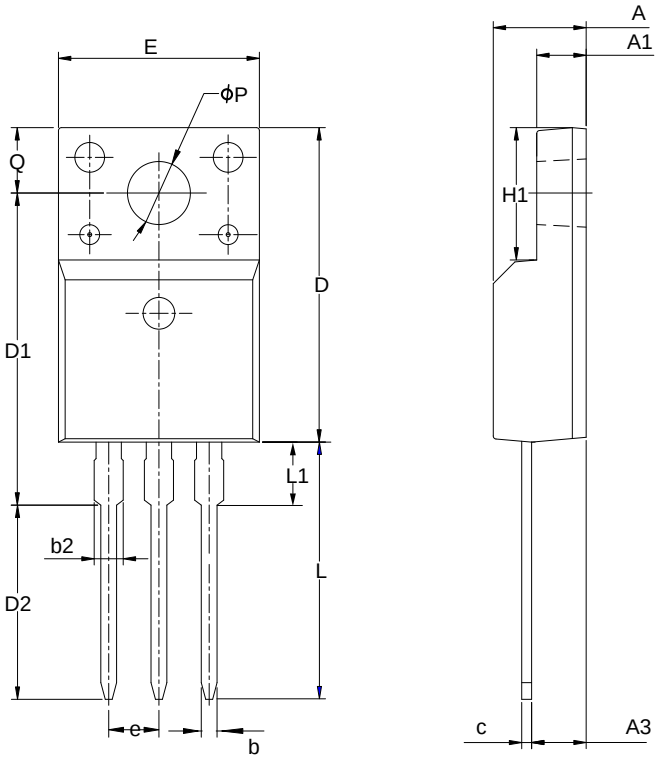
$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



PACKAGE OUTLINE

TO-220F-3L

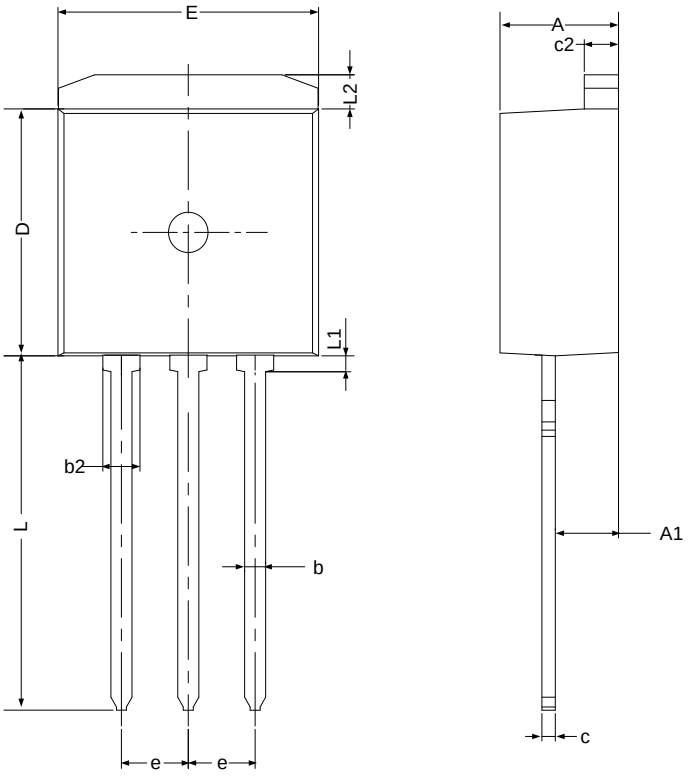
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-262-3L

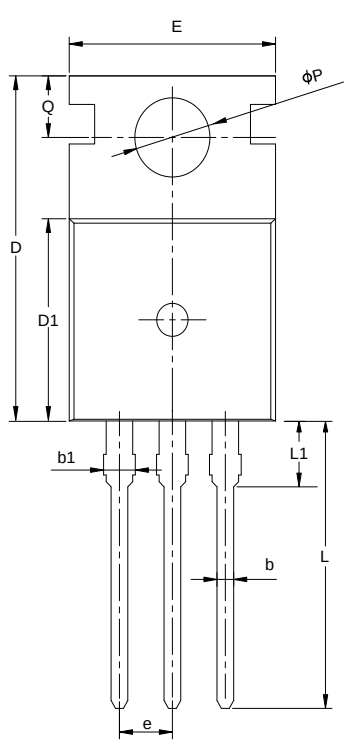
UNIT: mm

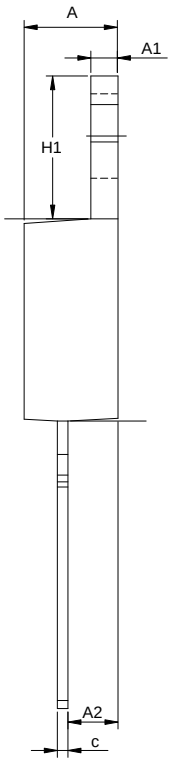


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.90
b2	1.20	—	1.50
c	0.34	—	0.65
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	—	—	0.75
L2	1.12	—	1.42

PACKAGE OUTLINE(CONTINUED)

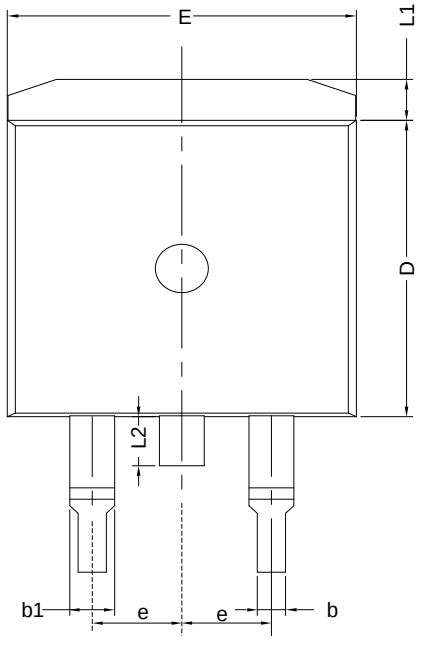
TO-220-3L **UNIT: mm**

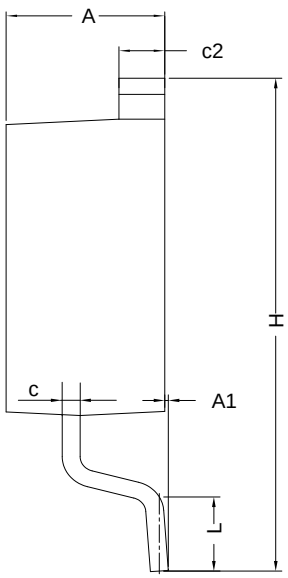




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-263-2L **UNIT: mm**





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

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- **The instructions are subject to change without notice！ Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
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Rev.: 2.5

Revision History:

1. Update the template of the datasheet

Rev.: 2.4

Revision History:

1. Add another solid figure of TO-220F-3L
2. Update the package outline of TO-262-3L

Rev.: 2.3

Revision History:

1. Modify the Electrical characteristics

Rev.: 2.2

Revision History:

1. Modify the package information of TO-220F-3L; Modify the package information of TO-220-3L

Rev.: 2.1

Revision History:

1. Modify the thermal characteristics

Rev.: 2.0

Revision History:

1. Modify the ordering information

Rev.: 1.9

Revision History:

1. Modify the ordering information

Rev.: 1.8

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.7

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.6
Revision History:
1. Add the package of TO-263-2L

Rev.: 1.5
Revision History:
1. Add the package of TO-262-3L

Rev.: 1.4
Revision History:
1. Modify the values of Trr and Qrr

Rev.: 1.3
Revision History:
1. Add the halogen free information of SVF10N65F

Rev.: 1.2
Revision History:
1. Modify “PACKAGE OUTLINE”

Rev.: 1.1
Revision History:
1. Modify “ELECTRICAL CHARACTERISTICS”

Rev.: 1.0
Revision History:
1. Original