

18A, 650V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF18N65EFJH is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

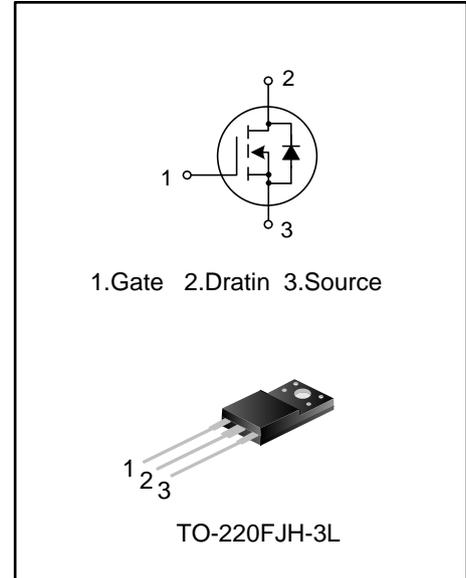
- ◆ 18A, 650V, $R_{DS(on)(typ.)}=0.48\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability
- ◆ 100% avalanche tested
- ◆ Pb-free lead plating
- ◆ RoHS compliant

KEY PERFORMANCE PARAMETERS

| Characteristics | Ratings | Unit |
|--------------------|---------|----------|
| V_{DS} | 650 | V |
| $V_{GS(th)}$ | 2.0~4.0 | V |
| $R_{DS(on), max.}$ | 0.55 | Ω |
| $I_{D,pulse}$ | 72 | A |
| $Q_{g,typ.}$ | 45 | nC |

ORDERING INFORMATION

| Part No. | Package | Marking | Hazardous Substance Control | Packing Type |
|--------------|--------------|-----------|-----------------------------|--------------|
| SVF18N65EFJH | TO-220FJH-3L | 18N65EFJH | Halogen free | Tube |



ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

| Characteristics | Symbol | Test conditions | Ratings | | | Unit |
|--------------------------------------|----------------------|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Drain-Source Voltage | V _{DS} | -- | 650 | -- | -- | V |
| Gate-source Voltage (Static) | V _{GS} | -- | -20 | -- | 20 | V |
| Gate-source Voltage (Dynamic) | V _{GS} | AC(f>1Hz) | -30 | -- | 30 | V |
| Drain Current | I _D | T _C =25°C | -- | -- | 18 | A |
| | | T _C =100°C | -- | -- | 11 | A |
| Drain Current Pulsed (Note 1) | I _{DM} | T _C =25°C | -- | -- | 72 | A |
| Power Dissipation (Note 2) | P _D | T _C =25°C | -- | -- | 54 | W |
| Single Pulsed Avalanche Energy | E _{AS} | L=30mH, V _{DD} =100V, R _G =25Ω, starting temperature T _J =25°C | -- | -- | 1282 | mJ |
| Single Pulsed Current | I _{AS} | -- | -- | -- | 8.6 | A |
| Reverse Diode dv/dt | dv/dt | V _{DS} =0~400V, I _{SD} <=I _S , T _J =25°C | -- | -- | 4.5 | V/ns |
| MOSFET dv/dt Ruggedness | dv/dt | V _{DS} =0~480V | -- | -- | 50 | V/ns |
| Operation Junction Temperature Range | T _J | -- | -55 | -- | 150 | °C |
| Storage Temperature Range | T _{stg} | -- | -55 | -- | 150 | °C |
| Continuous Diode Forward Current | I _S | T _C =25°C,integral reverse P-N junction diode in the MOSFET | -- | -- | 18 | A |
| Diode Pulse Current | I _{S,pulse} | | -- | -- | 72 | A |
| Maximum Diode Commutation Speed | di/dt | V _{DS} =0~400V, I _{SD} <= I _S , T _J =25°C | -- | -- | 250 | A/μs |

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Test conditions | Ratings | | | Unit |
|---|-------------------|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Thermal Resistance, Junction-case, Bottom | R _{θJC} | -- | -- | -- | 2.3 | °C/W |
| Thermal Resistance, Junction-ambient | R _{θJA} | -- | -- | -- | 62.5 | °C/W |
| Soldering Temperature (SMD) | T _{sold} | 15 ⁺² ₋₀ sec, 1time | -- | -- | 260 | °C |

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Static characteristics

| Characteristics | Symbol | Test conditions | Ratings | | | Unit |
|---|---------------------|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Drain-source Breakdown Voltage | BV _{DSS} | V _{GS} =0V, I _D =250μA | 650 | -- | -- | V |
| Drain-source Leakage Current | I _{DSS} | V _{DS} =650V, V _{GS} =0V, T _J =25°C | -- | -- | 1.0 | μA |
| | | V _{DS} =650V, V _{GS} =0V, T _J =125°C | -- | 2.0 | -- | μA |
| Gate-source Leakage Current | I _{GSS} | V _{GS} =±30V, V _{DS} =0V | -- | -- | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{GS} =V _{DS} , I _D =250μA | 2.0 | -- | 4.0 | V |
| Static Drain-source On State Resistance | R _{DS(on)} | V _{GS} =10V, I _D =9.0A | -- | 0.48 | 0.55 | Ω |

Dynamic characteristics

| Characteristics | Symbol | Test conditions | Ratings | | | Unit |
|------------------------------|----------------------|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Input Capacitance | C _{iss} | f=1MHz, V _{GS} =0V, V _{DS} =25V | -- | 2338 | -- | pF |
| Output Capacitance | C _{oss} | | -- | 238 | -- | |
| Reverse Transfer Capacitance | C _{rss} | | -- | 7.0 | -- | |
| Turn-on Delay Time | t _{d(on)} | V _{DD} =325V, V _{GS} =10V, R _G =25Ω, I _D =18A (Notes 3,4) | -- | 38 | -- | ns |
| Turn-on Rise Time | t _r | | -- | 62 | -- | |
| Turn-off Delay Time | t _{d(off)} | | -- | 143 | -- | |
| Turn-off Fall Time | t _f | | -- | 67 | -- | |
| Total Gate Charge | Q _g | V _{DD} =520V, V _{GS} =10V, I _D =18A (Notes 3,4) | -- | 45 | -- | nC |
| Gate-source Charge | Q _{gs} | | -- | 15 | -- | |
| Gate-drain Charge | Q _{gd} | | -- | 14 | -- | |
| Gate-plateau Voltage | V _{plateau} | | -- | 6.0 | -- | V |

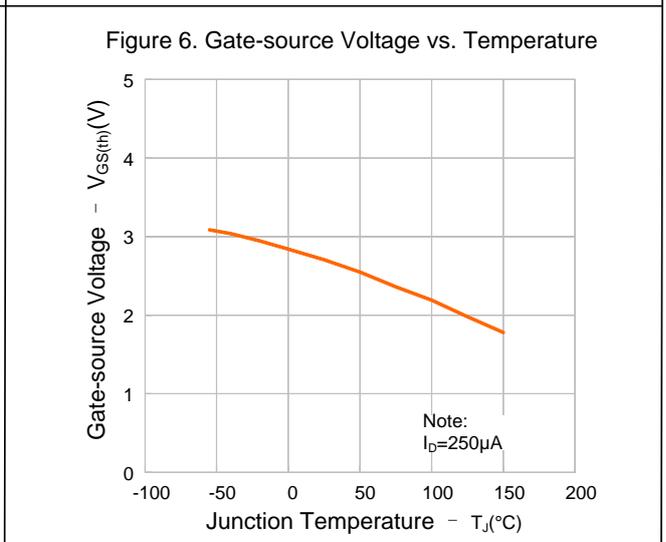
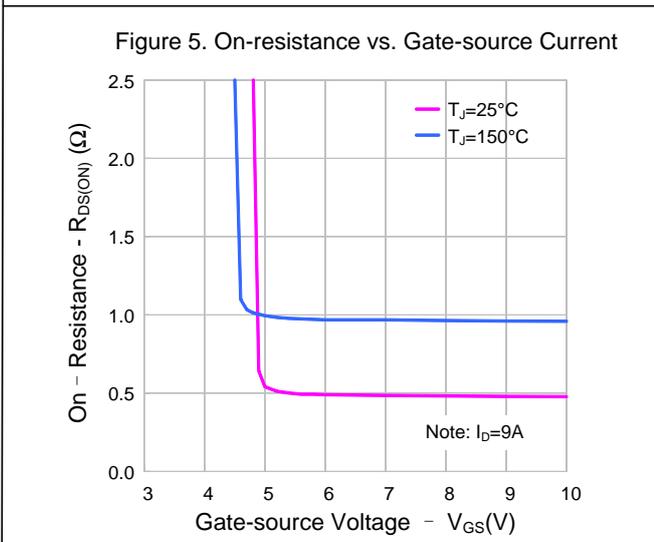
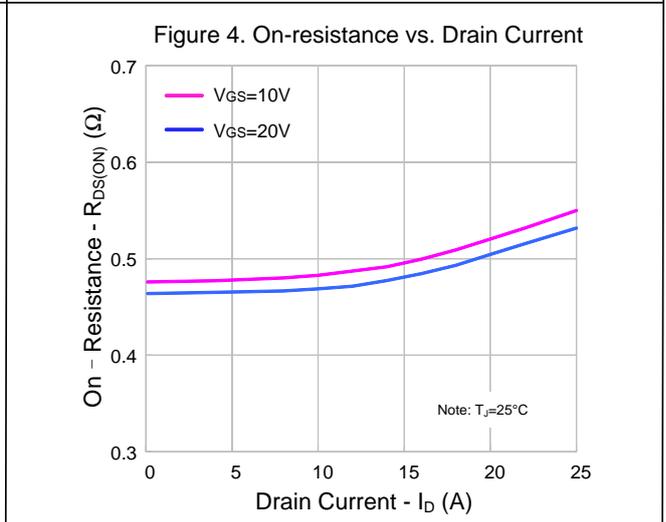
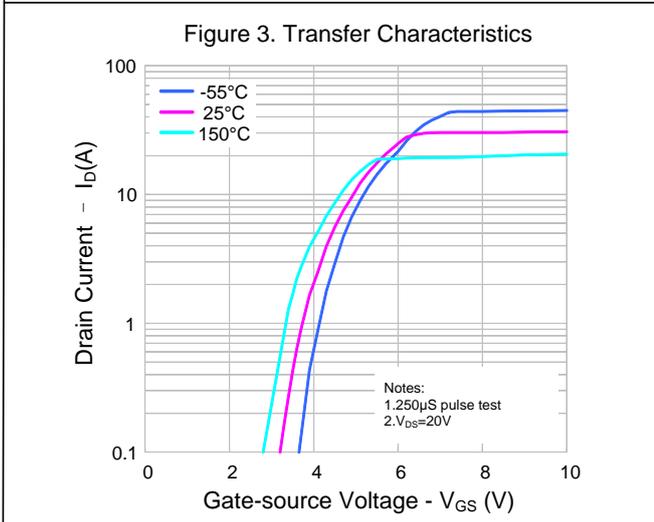
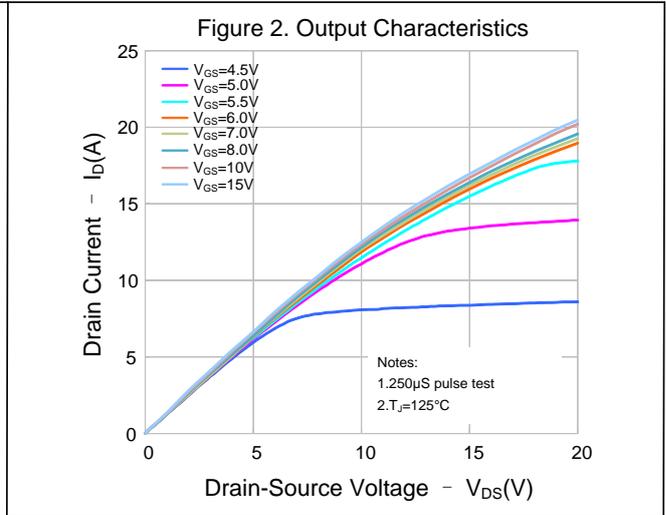
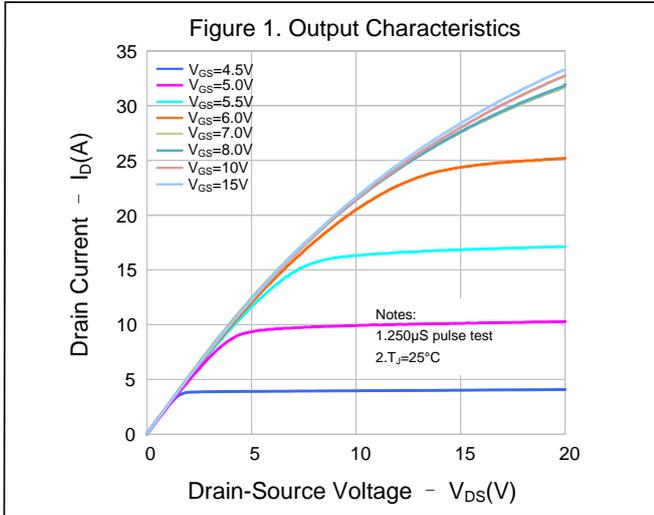
Reverse diode characteristics

| Characteristics | Symbol | Test conditions | Ratings | | | Unit |
|-------------------------------|------------------|--|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Diode Forward Voltage | V _{SD} | I _S =18A, V _{GS} =0V | -- | -- | 1.4 | V |
| Reverse Recovery Time | T _{rr} | I _S =18A, V _{GS} =0V, dI _F /dt=100A/μs (Note 3) | -- | 573 | -- | ns |
| Reverse Recovery Charge | Q _{rr} | | -- | 7.1 | -- | μC |
| Reverse Recovery Peak Current | I _{rrm} | | -- | 26 | -- | A |

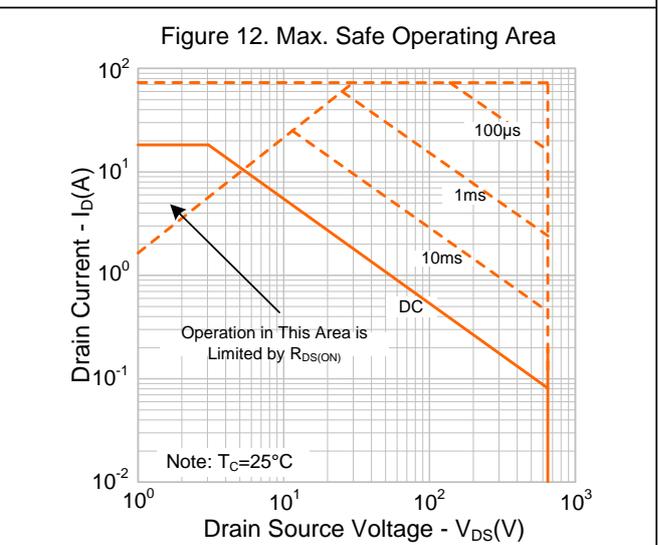
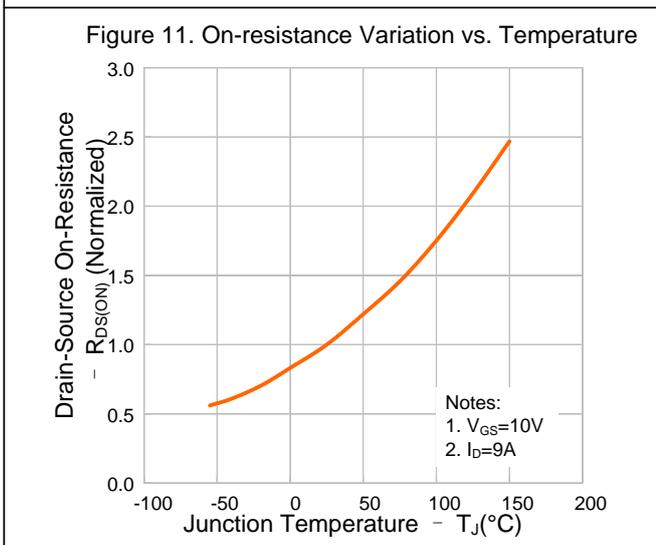
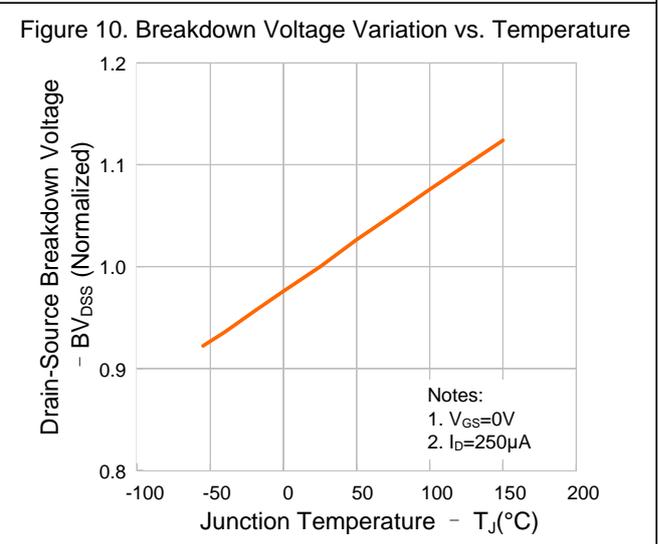
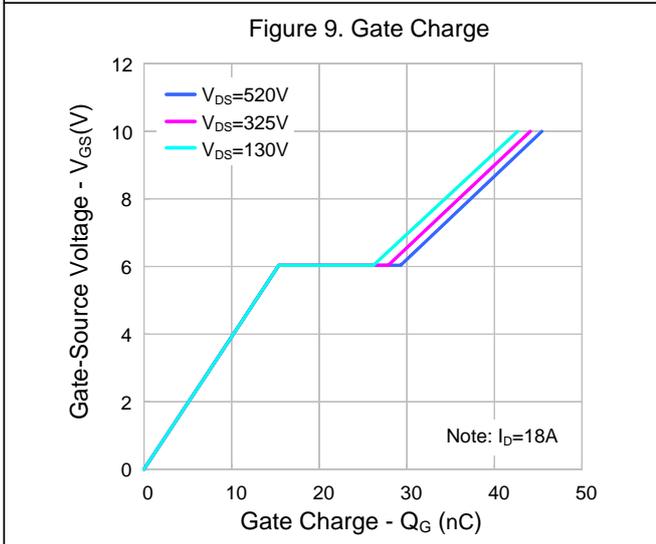
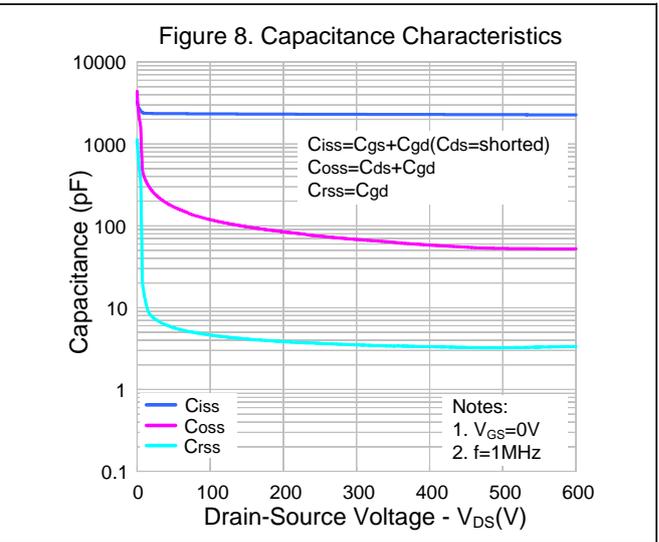
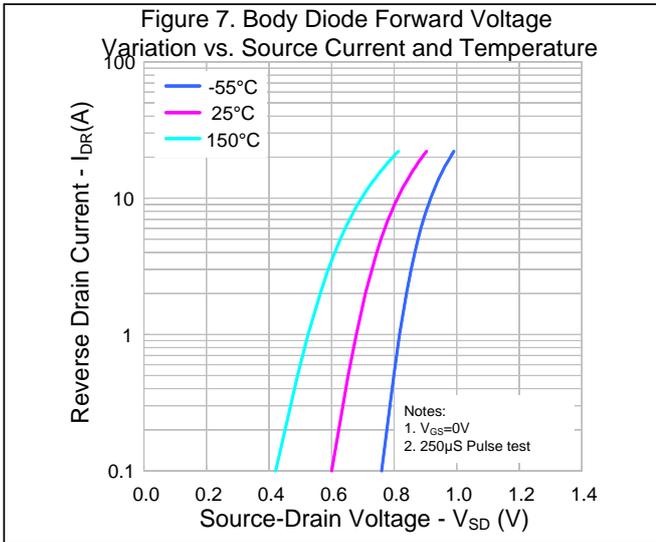
Notes:

1. Pulse time 5μs;
2. The dissipation power will change with temperature, derating above 25°C: 0.43W/°C;
3. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
4. Essentially independent of operating temperature.

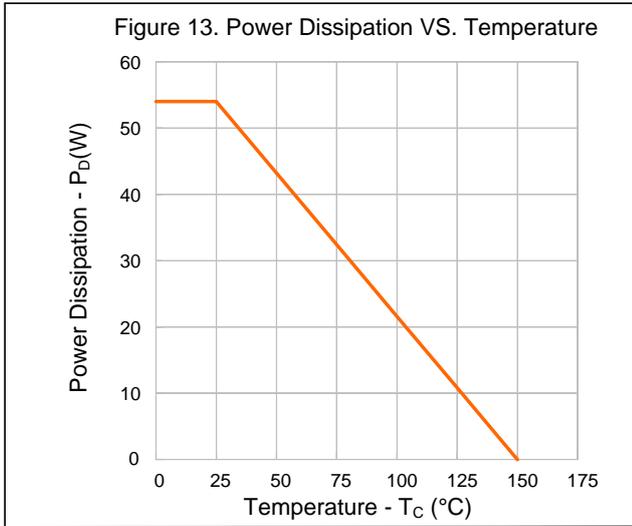
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONTINUED)

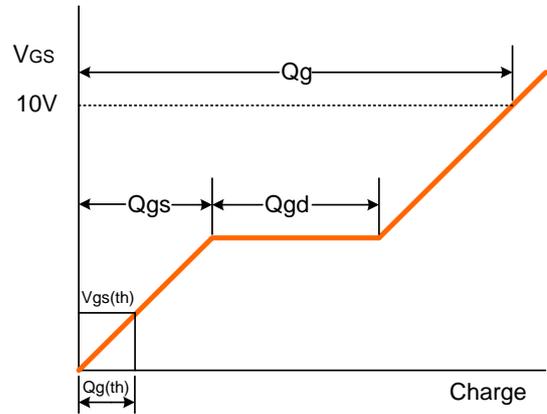
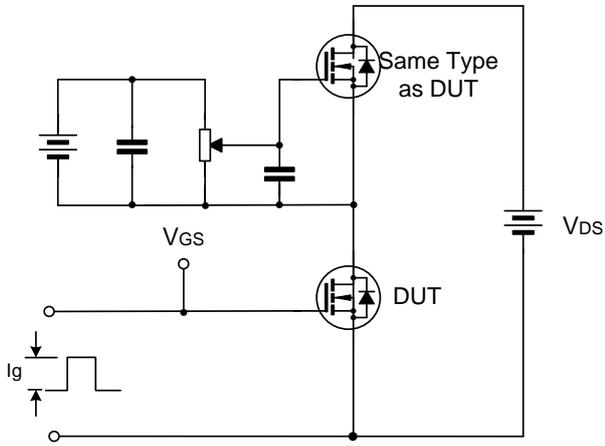


TYPICAL CHARACTERISTICS(CONTINUED)

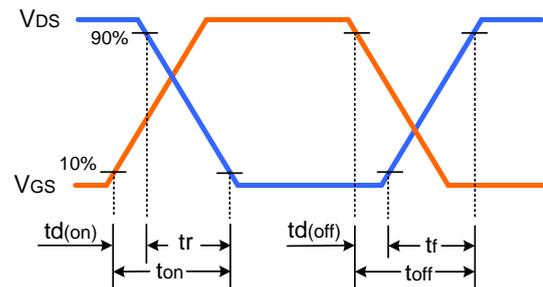
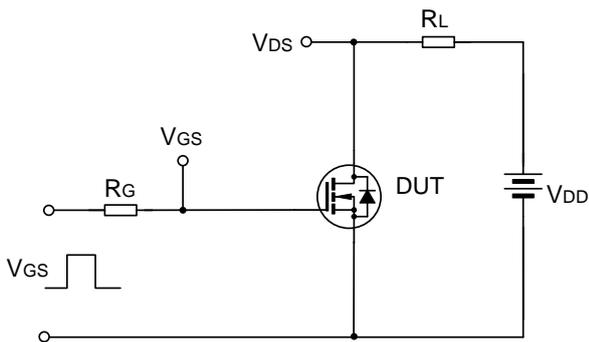


TYPICAL TEST CIRCUIT

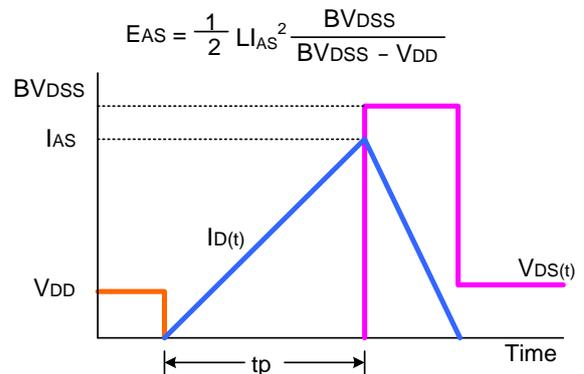
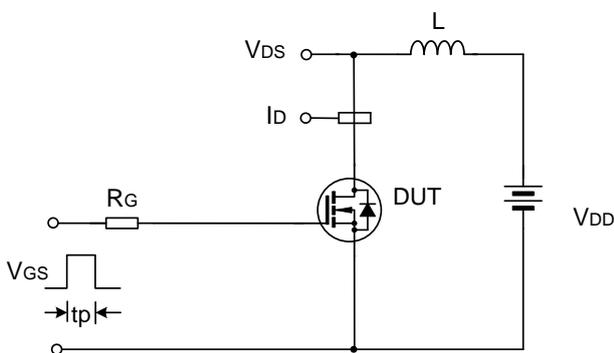
Gate Charge Test Circuit & Waveform



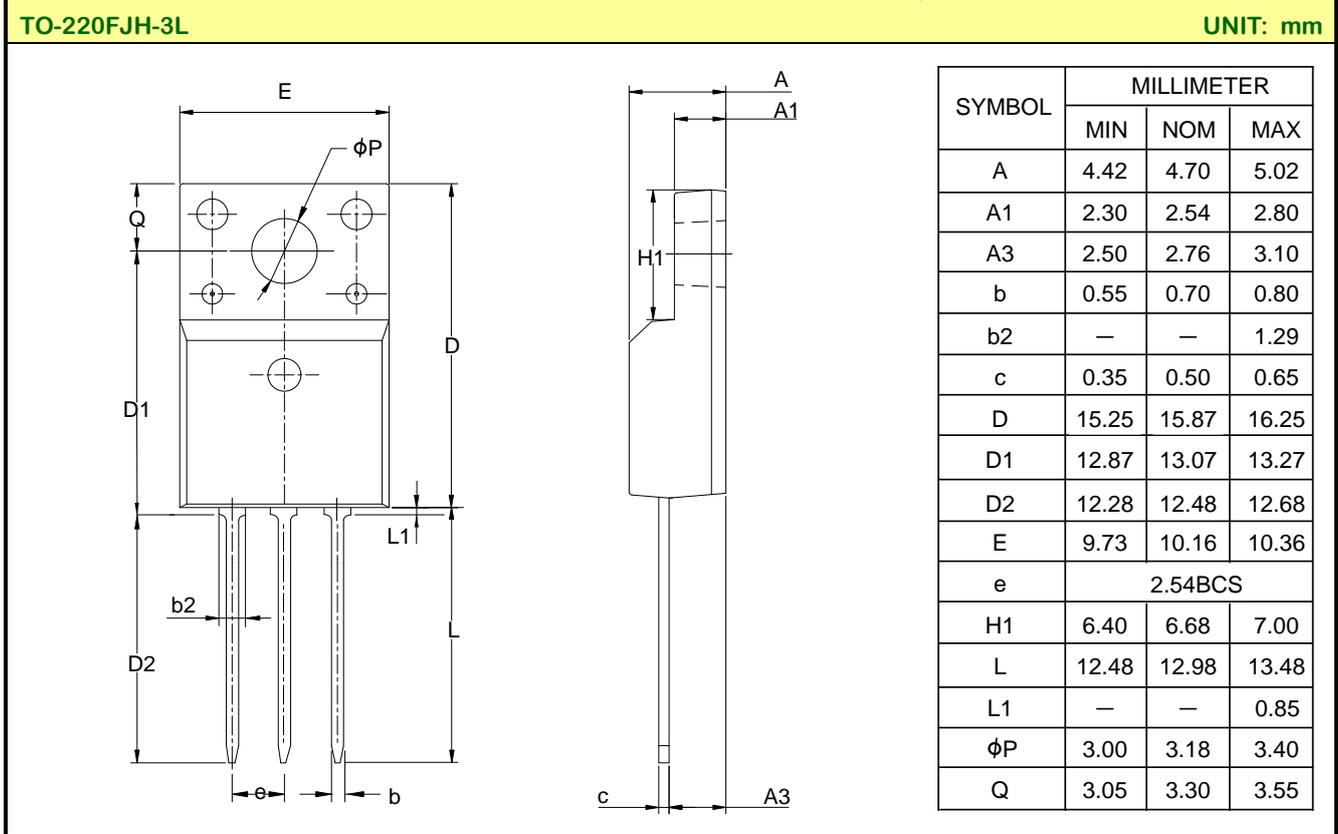
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE



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Rev.: 1.0

Revision History:

1. First release
