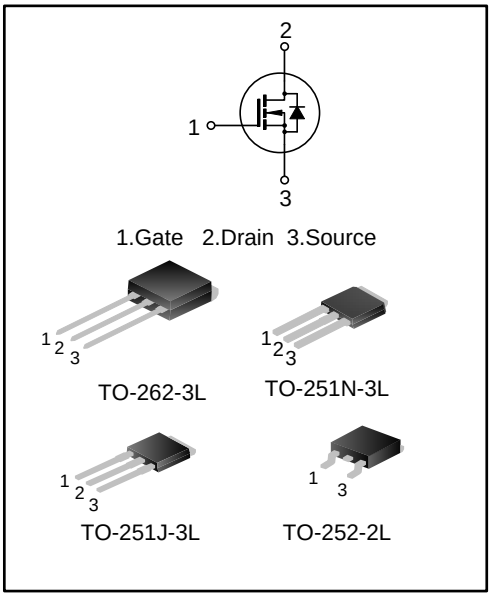
6A, 700V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF6N70MJG/D/K/N is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 6A,700V,$R_{DS(on(typ.)}$=1.35Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF6N70MJG	TO-251J-3L	SVF6N70MJG	Halogen free	Tube
SVF6N70DTR	TO-252-2L	SVF6N70D	Halogen free	Tape & Reel
SVF6N70K	TO-262-3L	SVF6N70K	Pb free	Tube
SVF6N70MN	TO-251N-3L	6N70MN	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (Tc=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings		Unit
			SVF6N70MJG/D/N	SVF6N70K	
Drain-Source Voltage		V_{DS}	700		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	6.0		A
	T_C=100°C		3.8		
Drain Current Pulsed		I_{DM}	24.0		A
Power Dissipation(T_C=25°C)		P_D	128	130	W
-Derate above 25°C			1.02	1.04	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	463		mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF6N70MJG/D/N	SVF6N70K	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.98	0.96	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	700	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=700V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.0A	--	1.35	1.7	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	770	--	pF
Output Capacitance	C_{oss}		--	90	--	
Reverse Transfer Capacitance	C_{rss}		--	8.2	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=350V,I_D=6.0A, R_G=25Ω (Note 2,3)	--	14	--	ns
Turn-on Rise Time	t_r		--	29	--	
Turn-off Delay Time	$t_{d(off)}$		--	52	--	
Turn-off Fall Time	t_f		--	30	--	
Total Gate Charge	Q_g	V_{DS}=560V,I_D=6.0A, V_{GS}=10V (Note 2,3)	--	21	--	nC
Gate-Source Charge	Q_{gs}		--	5.6	--	
Gate-Drain Charge	Q_{gd}		--	10	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	6.0	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	24.0	
Diode Forward Voltage	V_{SD}	I_S=6.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=6.0A,V_{GS}=0V,	--	465	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs(Note 2)	--	3	--	μC

Notes:

1. L=30mH, I_{AS}=5.00A,V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

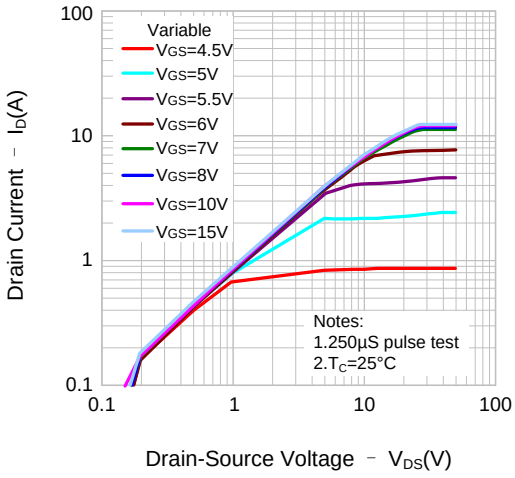


Figure 2. Transfer Characteristics

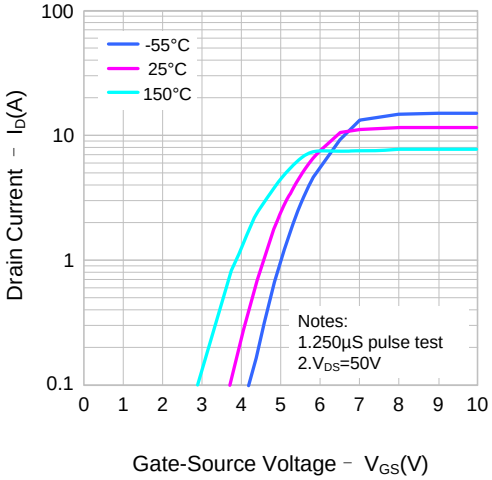


Figure 3. On-Resitance Variation vs. Drain Current

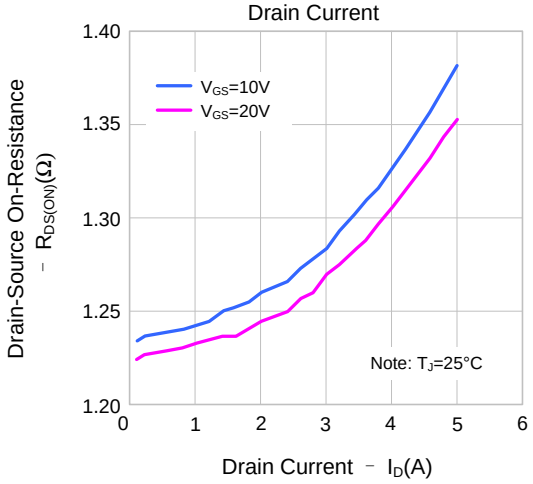


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

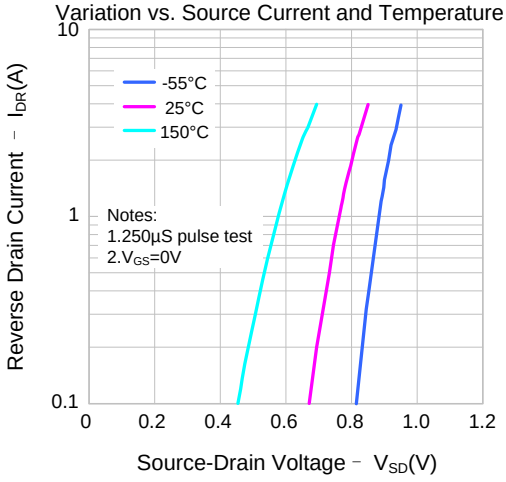


Figure 5. Capacitance Characteristics

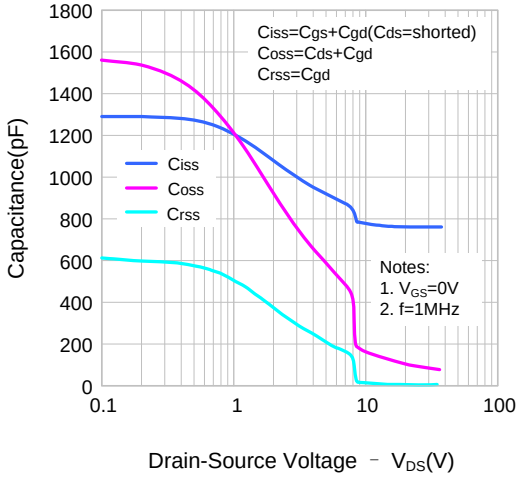
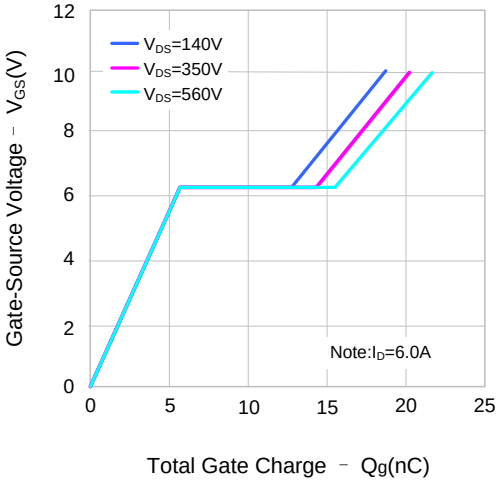


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

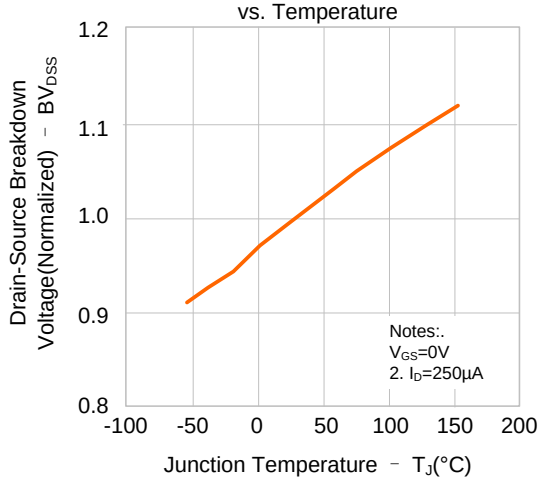


Figure 8. On-resistance Variation vs. Temperature

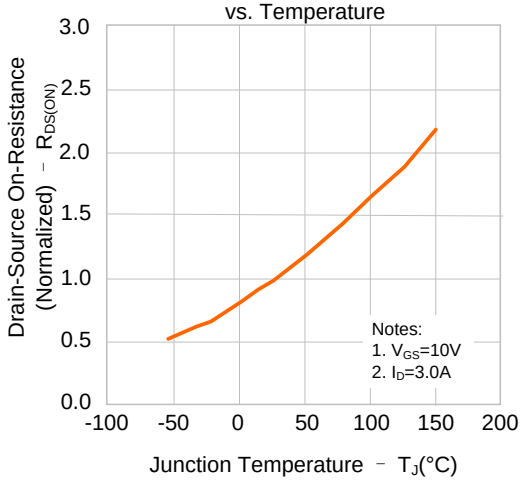


Figure 9-1. Max. Safe Operating Area(SVF6N70MJG/D/N)

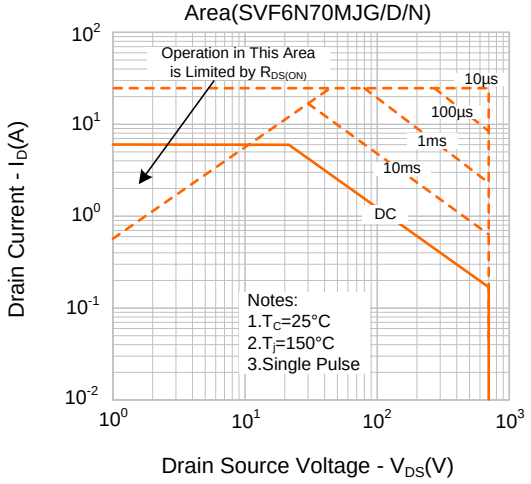


Figure 9-2. Max. Safe Operating Area(SVF6N70K)

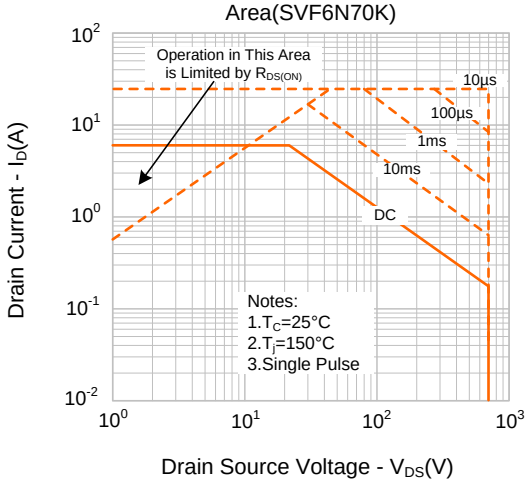
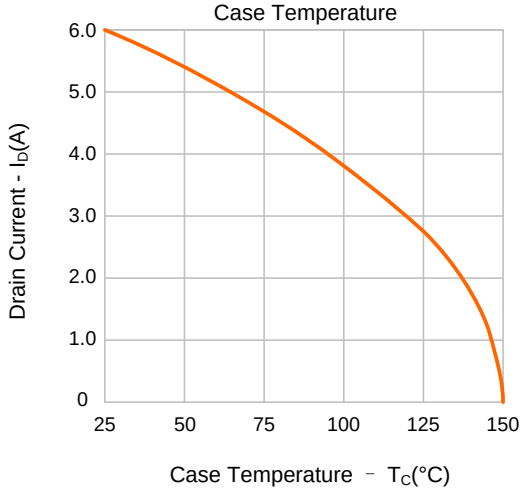
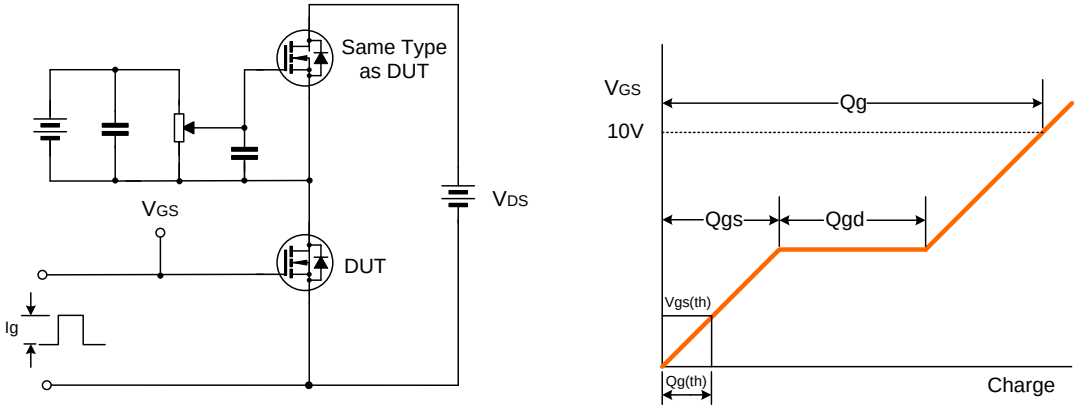


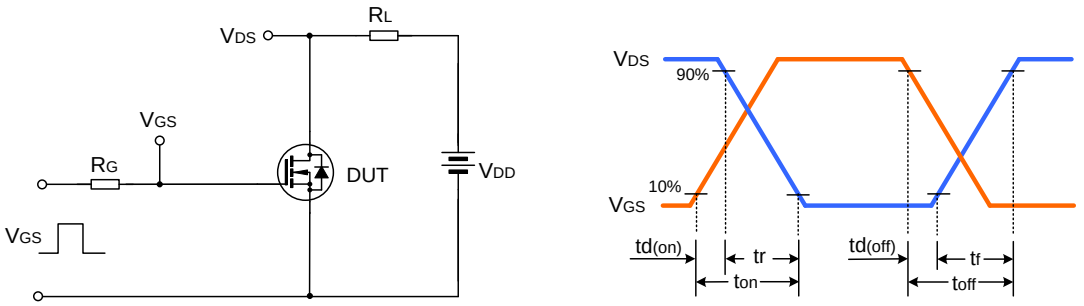
Figure 10. Maximum Drain Current vs. Case Temperature



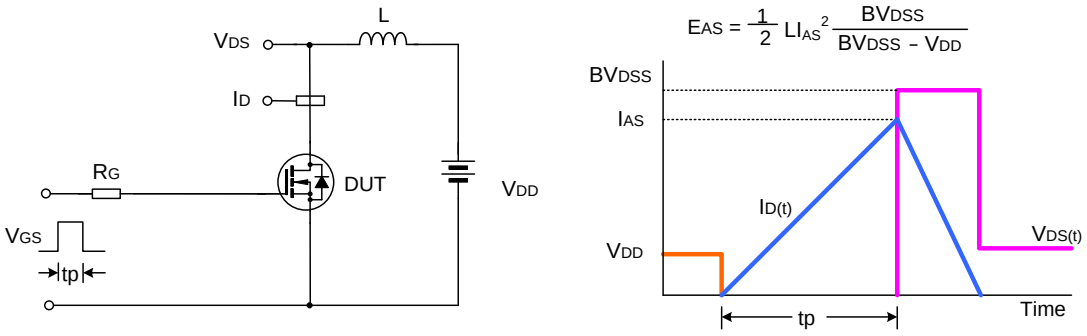
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

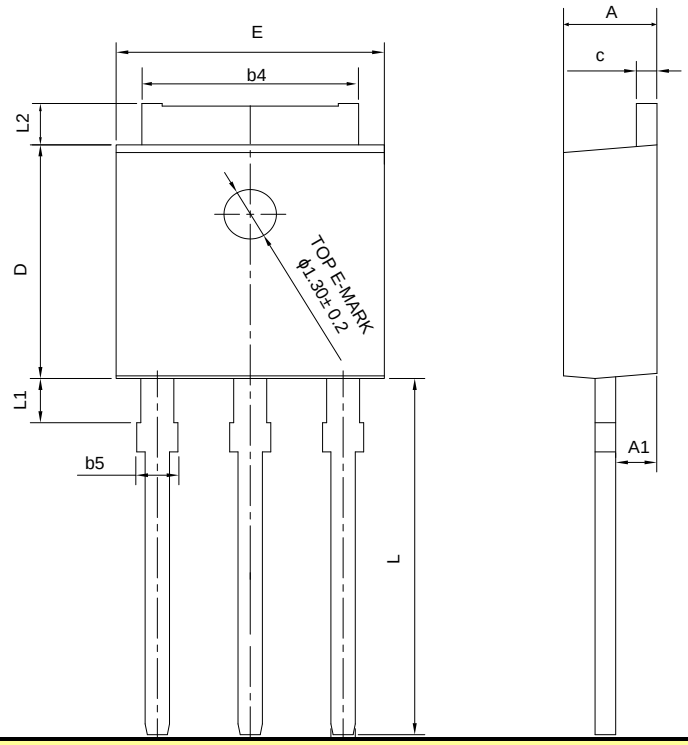


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-251J-3L

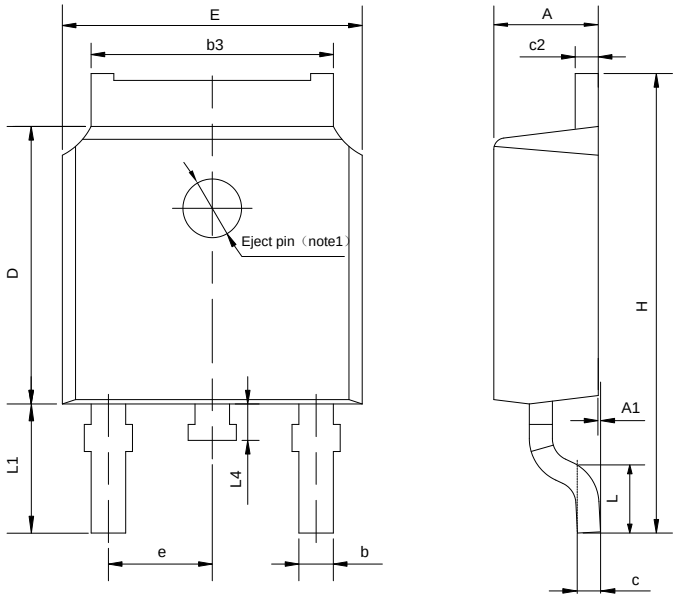
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	—	0.89
b4	4.95	5.33	5.46
b5	—	—	1.05
c	0.46	—	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	—	1.50
L2	0.89	—	1.27

TO-252-2L

UNIT: mm



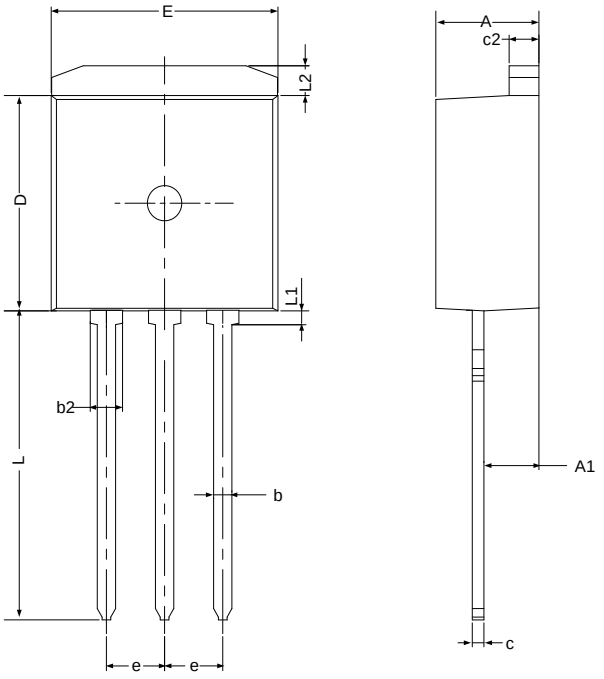
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE(CONTINUED)

TO-262-3L

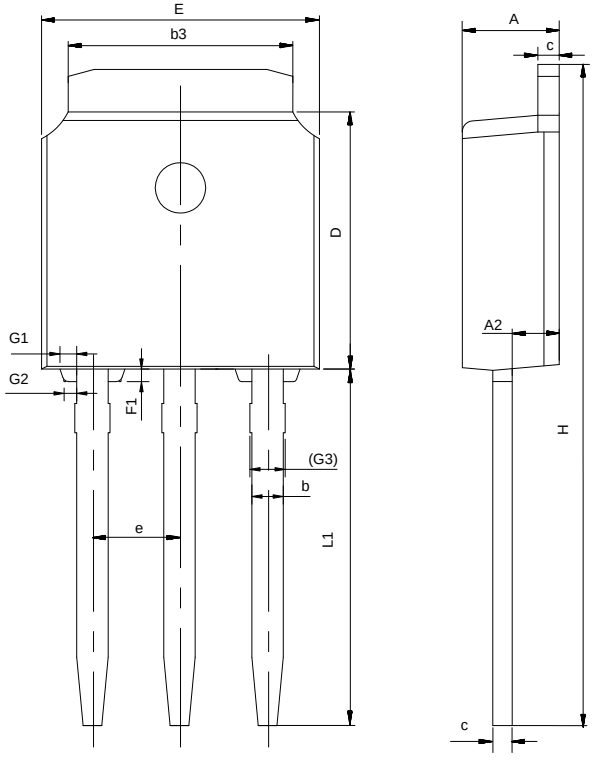
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.90
b2	1.20	—	1.50
c	0.34	—	0.65
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	—	—	0.75
L2	1.12	—	1.42

TO-251N-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A2	0.97	1.07	1.17
b	0.58	0.68	0.80
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.286 BSC		
F1	0.20	0.30	0.40
G1	0.30	0.40	0.50
G2	0.20	0.30	0.40
G3	0.60	0.74	0.88
H	16.02	16.52	17.02
L1	9.10	9.40	9.70

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Rev.: 2.9

Revision History:

1. Deleted NOMENCLATURE
2. Modify Important notice

Rev.: 2.8

Revision History:

1. Modify the package outline of TO-251N-3L

Rev.: 2.7

Revision History:

1. Modify the package outline of TO-251N-3L
2. Modify ORDERING INFORMATION
3. Modify Important notice

Rev.: 2.6

Revision History:

1. Update the package outline of TO-251N-3L
2. Update the package outline of TO-262-3L
3. Update TYPICAL TEST CIRCUIT

Rev.: 2.5

Revision History:

1. Add the package outline of TO-251N-3L

Rev.: 2.4

Revision History:

1. Update the package outline of TO-251J-3L
2. Modify ordering information

Rev.: 2.3

Revision History:

1. Modify the package information of TO-252-2L

Rev.: 2.2

Revision History:

1. Modify the electrical characteristics and the typical characteristics

Rev.: 2.1

Revision History:

1. Modify the thermal characteristics

Rev.: 2.0

Revision History:

1. Modify the curve of SOA

Rev.: 1.9

Revision History:

1. Add the package of TO-262-3L

Rev.: 1.8

Revision History:

1. Modify the marking and package outline of TO-251J-3L

Rev.: 1.7

Revision History:

1. Modify the ordering information

Rev.: 1.6

Revision History:

1. Modify the ordering information

Rev.: 1.5

Revision History:

1. Change the schematic diagram of MOS; Add the value of Rg

Rev.: 1.4

Revision History:

1. Delete the package of TO-220F-3L

Rev.: 1.3

Revision History:

1. Add the package of TO-252-2L

Rev.: 1.2

Revision History:

1. Modify the values of T_{rr} and Q_{rr}

Rev.: 1.1

Revision History:

1. Add the package of TO-251J-3L

Rev.: 1.0

Revision History:

1. First release