

6A, 800V N-CHANNEL MOSFET

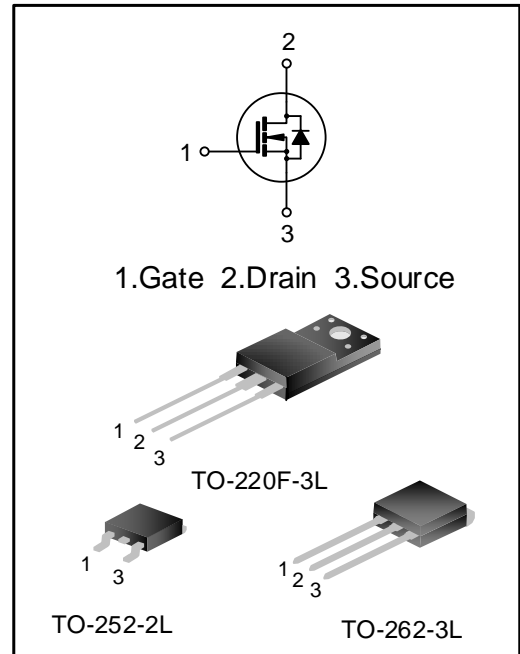
GENERAL DESCRIPTION

SVF6N80AD(K)(F) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 6A,800V, $R_{DS(on)(typ.)}=1.9\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF6N80ADTR	TO-252-2L	6N80AD	Halogen free	Tape&Reel
SVF6N80AK	TO-262-3L	SVF6N80AK	Pb free	Tube
SVF6N80AF	TO-220F-3L	SVF6N80AF	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Ratings			Unit
		SVF6N80AD	SVF6N80AK	SVF6N80AF	
Drain-Source Voltage	V _{DS}	800			V
Gate-Source Voltage	V _{GS}	±30			V
Drain Current	I _D	T _C =25°C			A
		T _C =100°C			
Drain Current Pulsed	I _{DM}	24			A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	160	190	41	W
		1.3	1.5	0.33	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	L=10mH			mJ
		L=30mH			
Reverse Diode dv/dt (Note 2)	dv/dt	4.5			V/ns
MOSFET dv/dt Ruggedness (Note 3)	dv/dt	50			V/ns
Operation Junction Temperature Range	T _J	-55~+150			°C
Storage Temperature Range	T _{stg}	-55~+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF6N80AD	SVF6N80AK	SVF6N80AF	
Thermal Resistance, Junction-to-Case	R _{θJC}	0.78	0.66	3.05	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.0	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	800	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =800V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.0A	--	1.9	2.2	Ω
Gate resistance	R _g	f=1.0MHz	--	4.8	--	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	979	--	pF
Output Capacitance	C _{oss}		--	85	--	
Reverse Transfer Capacitance	C _{rss}		--	4.7	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =400V, I _D =6.0A, R _G =25Ω (Note 4,5)	--	12	--	ns
Turn-on Rise Time	t _r		--	24	--	
Turn-off Delay Time	t _{d(off)}		--	64	--	
Turn-off Fall Time	t _f		--	35	--	
Total Gate Charge	Q _g	V _{DS} =640V, I _D =6.0A, V _{GS} =10V (Note 4,5)	--	23	--	nC
Gate-Source Charge	Q _{gs}		--	7.0	--	
Gate-Drain Charge	Q _{gd}		--	8.8	--	

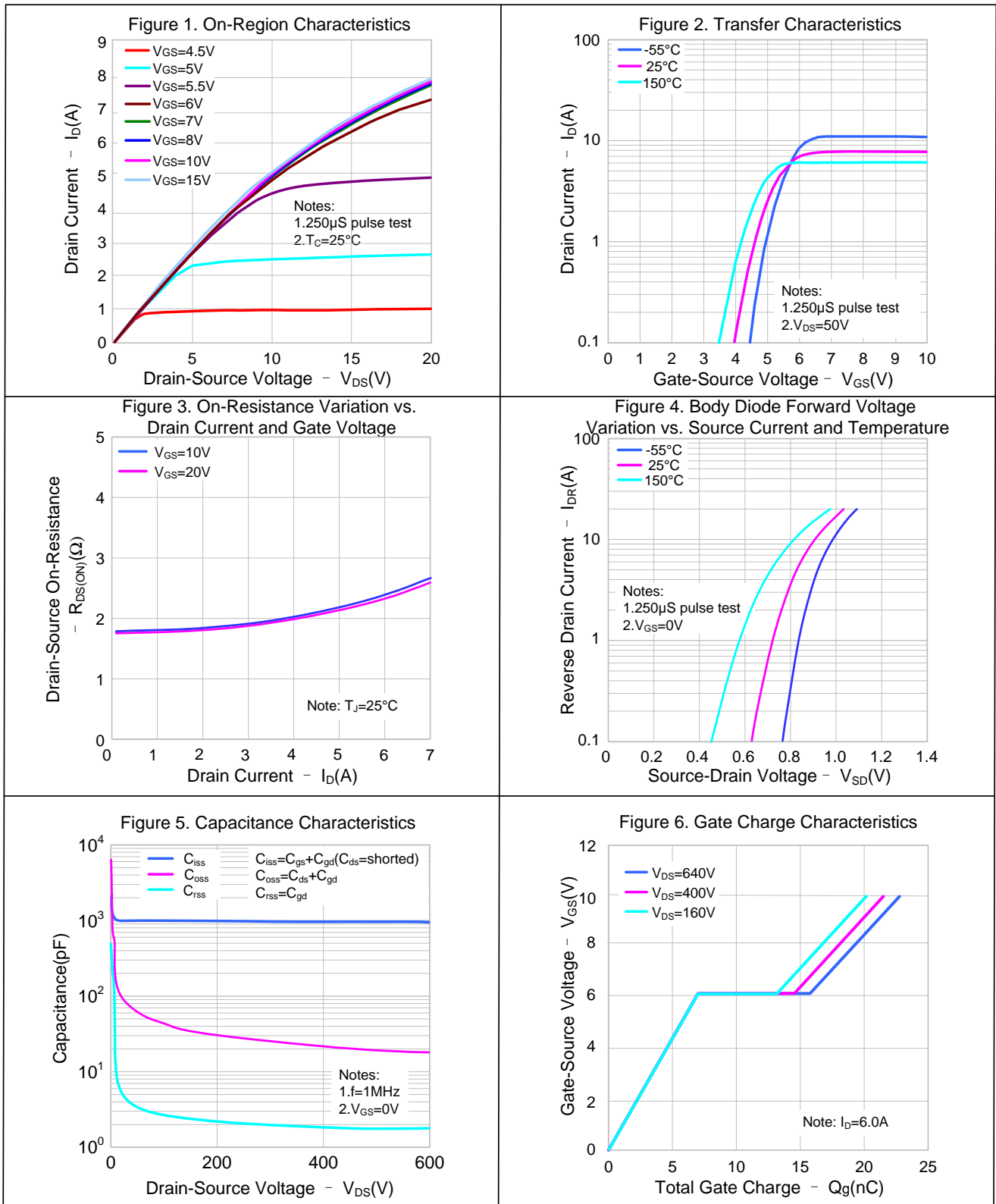
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	6.0	A
Pulsed Source Current	I _{SM}		--	--	24	
Diode Forward Voltage	V _{SD}	I _S =6.0A, V _{GS} =0V	--	--	1.4	V
Reverse Recovery Time	T _{rr}	I _S =6.0A, V _{GS} =0V, dI _F /dt=100A/μs (Note 4)	--	566	--	ns
Reverse Recovery Charge	Q _{rr}		--	3.7	--	μC

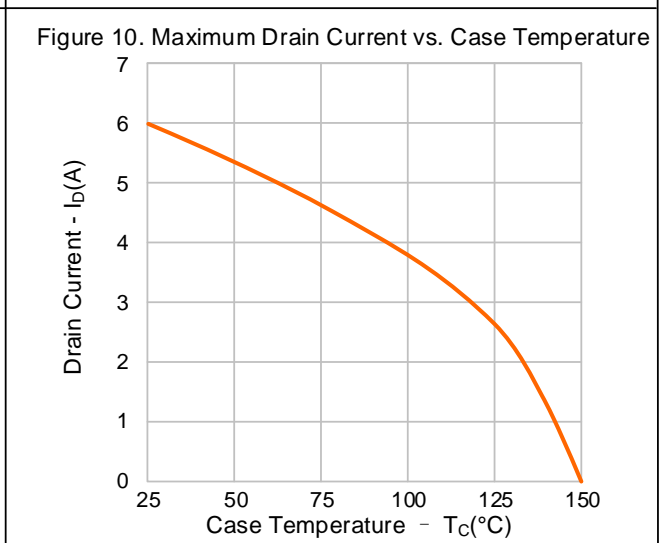
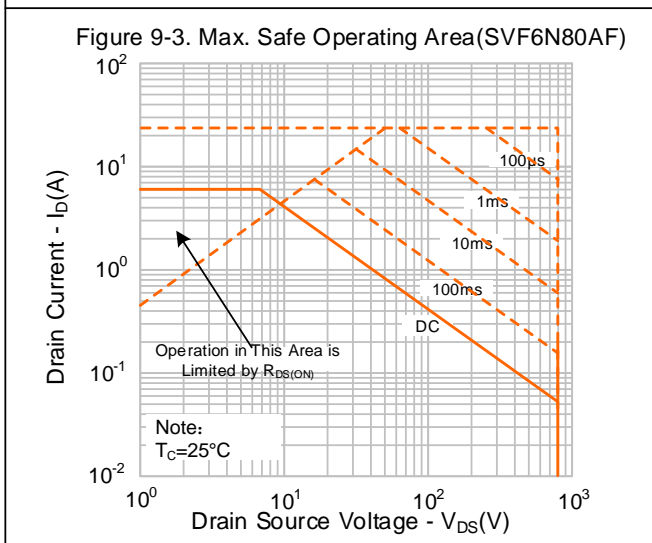
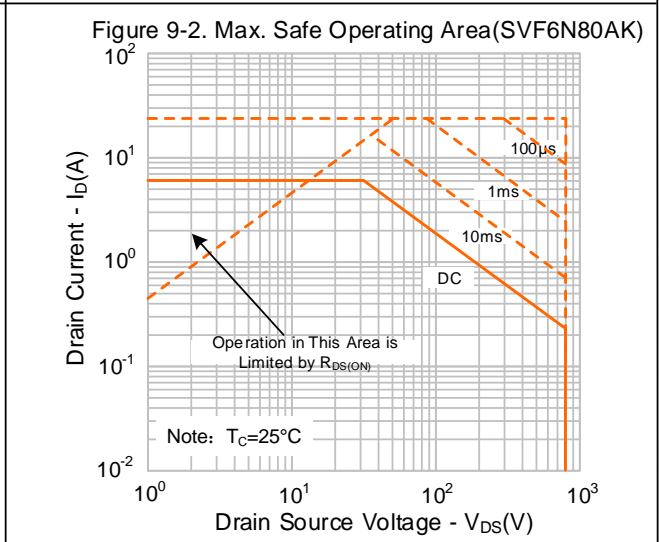
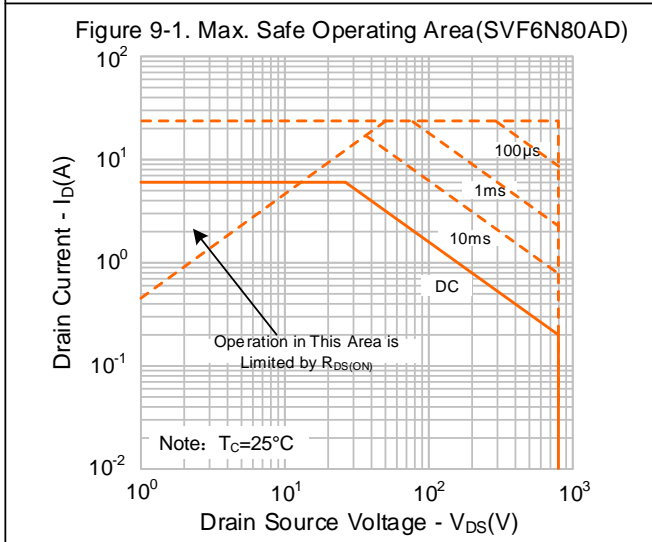
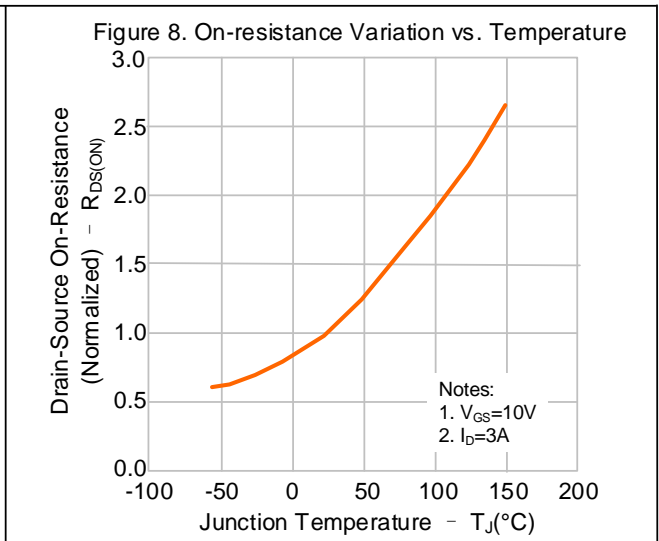
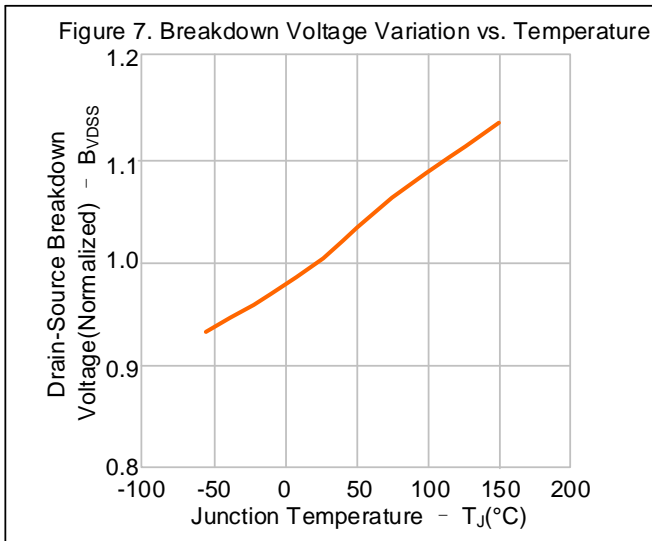
Notes:

- V_{DD}=80V, R_G=25Ω, starting T_{B,JB}=25°C;
- V_{DS}=0~400V, I_{SD}≤6.0A, T_J=25°C;
- V_{DS}=0~480V;
- Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
- Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

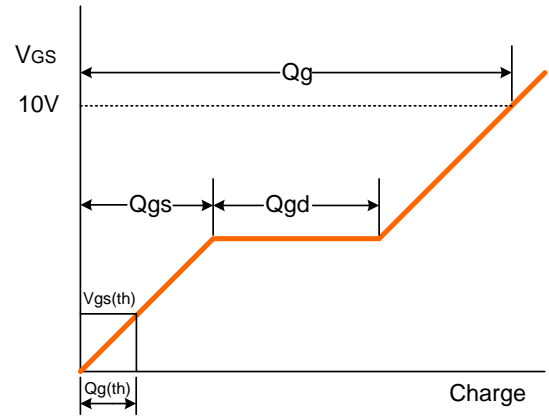
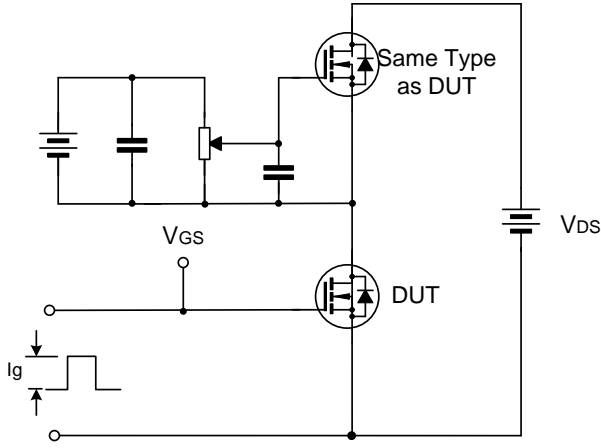


TYPICAL CHARACTERISTICS(CONTINUED)

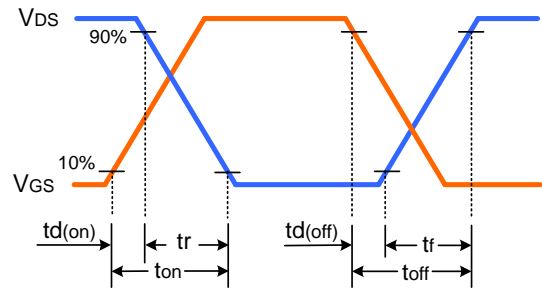
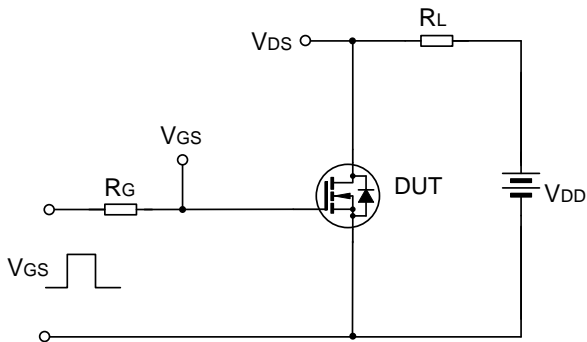


TYPICAL TEST CIRCUIT

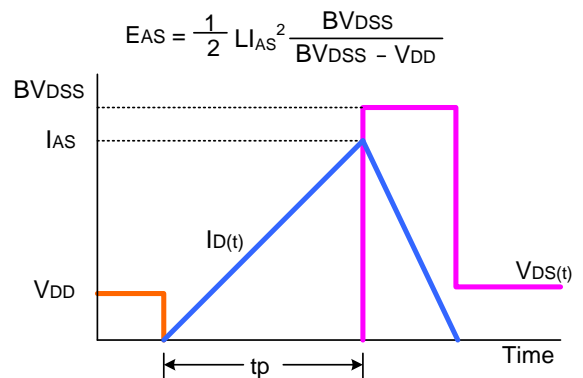
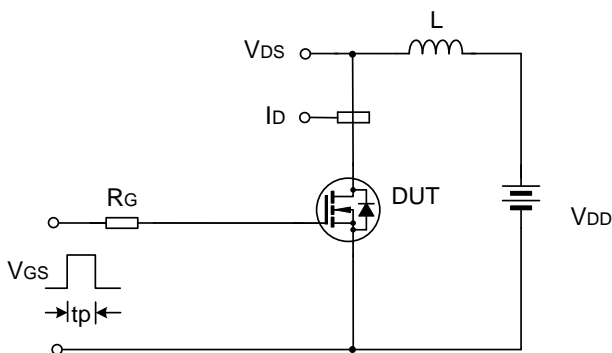
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



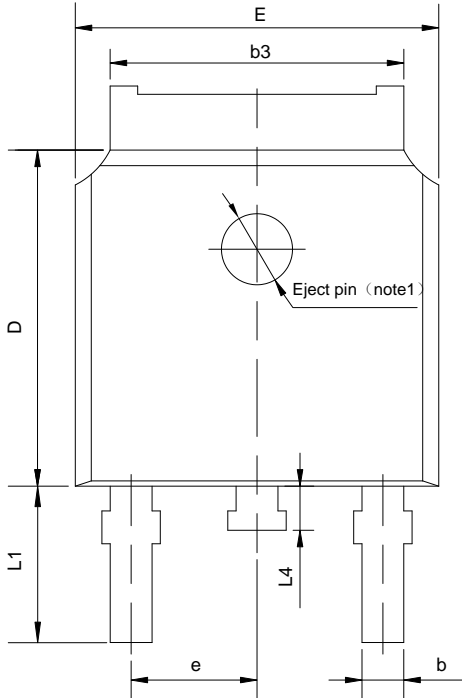
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

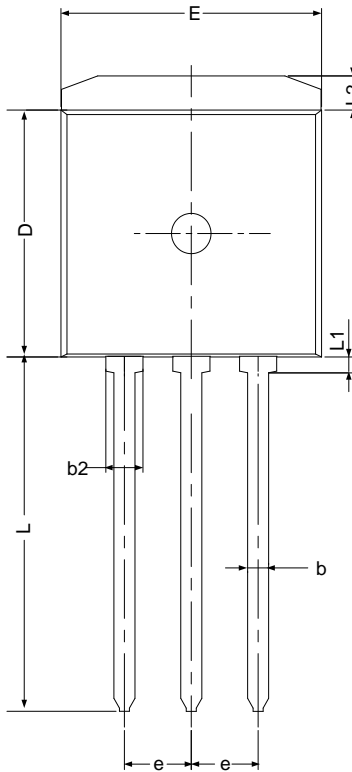


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-262-3L

UNIT: mm

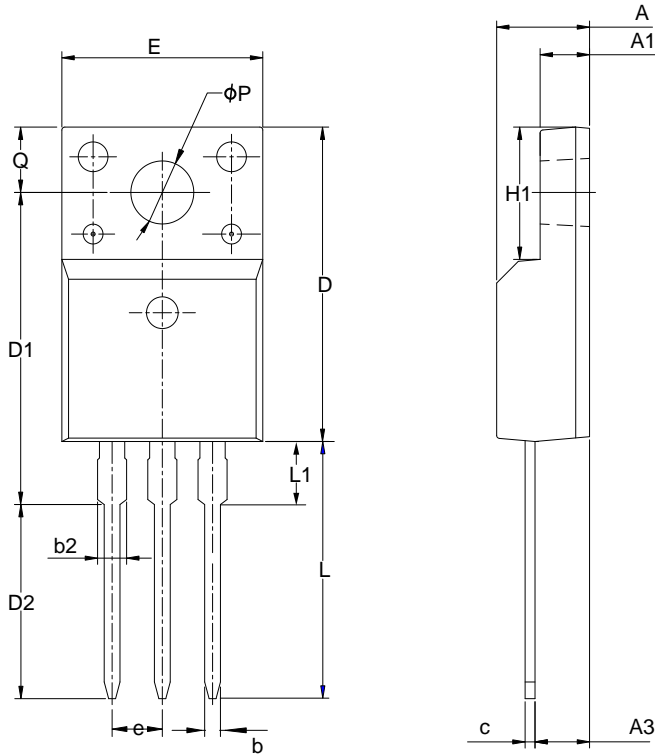


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.90
b2	1.20	—	1.50
c	0.34	—	0.65
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	—	—	0.75
L2	1.12	—	1.42

PACKAGE OUTLINE(CONTINUED)

TO-220F-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
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Rev.: 1.2

Revision History:

1. Add TO-220F-3L package
 2. Update the curve
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Rev.: 1.1

Revision History:

1. Update the template of datasheet
-

Rev.: 1.0

Revision History:

1. First release
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