

9A, 900V N-CHANNEL MOSFET

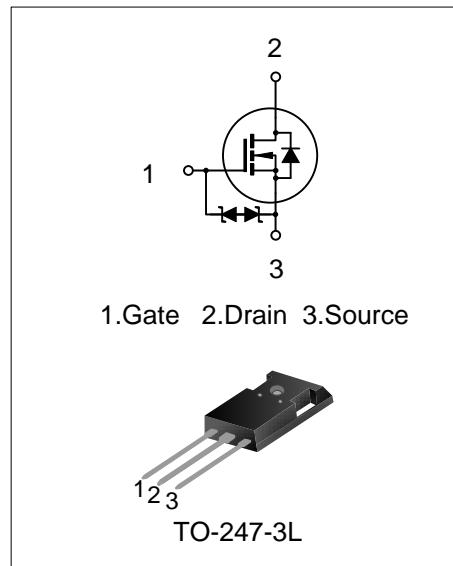
DESCRIPTION

SVF3878P7 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 9A, 900V, $R_{DS(on)}(typ.)=1.0\Omega @ V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF3878P7	TO-247-3L	3878	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, $T_A=25^\circ C$)

Characteristics		Symbol	Ratings		Unit
Drain-Source Voltage		V_{DS}	900		V
Gate-Source Voltage		V_{GS}	± 30		V
Drain Current	$T_C=25^\circ C$	I_D	9.0		A
	$T_C=100^\circ C$		5.7		
Drain Current Pulsed		I_{DM}	27.0		A
Power Dissipation ($T_C=25^\circ C$) -Derate above $25^\circ C$		P_D	150		W
			1.2		
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	966		mJ
Operation Junction Temperature Range		T_J	-55~+150		°C
Storage Temperature Range		T_{stg}	-55~+150		°C



THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.83	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^\circ C$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	900	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=900V, V_{GS}=0V$	--	--	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	± 10.0	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.5	--	4.5	V
On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.5A$	--	1.0	1.28	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	--	2009	--	pF
Output Capacitance	C_{oss}		--	208	--	
Reverse Transfer Capacitance	C_{rss}		--	47	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=400V, R_G=25\Omega, I_D=4.0A$ (Note2, 3)	--	22	--	ns
Turn-on Rise Time	t_r		--	28	--	
Turn-off Delay Time	$t_{d(off)}$		--	84	--	
Turn-off Fall Time	t_f		--	30	--	
Total Gate Charge	Q_g	$V_{DD}=450V, V_{GS}=10V, I_D=9.0A$ (Note 2, 3)	--	68	--	nC
Gate-Source Charge	Q_{gs}		--	10	--	
Gate-Drain Charge	Q_{gd}		--	39	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	I_s	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I_{SM}		--	--	27.0	
Diode Forward Voltage	V_{SD}	$I_s=9.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_s=9.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu S$ (Note2)	--	715	--	ns
Reverse Recovery Charge	Q_{rr}		--	6.5	--	

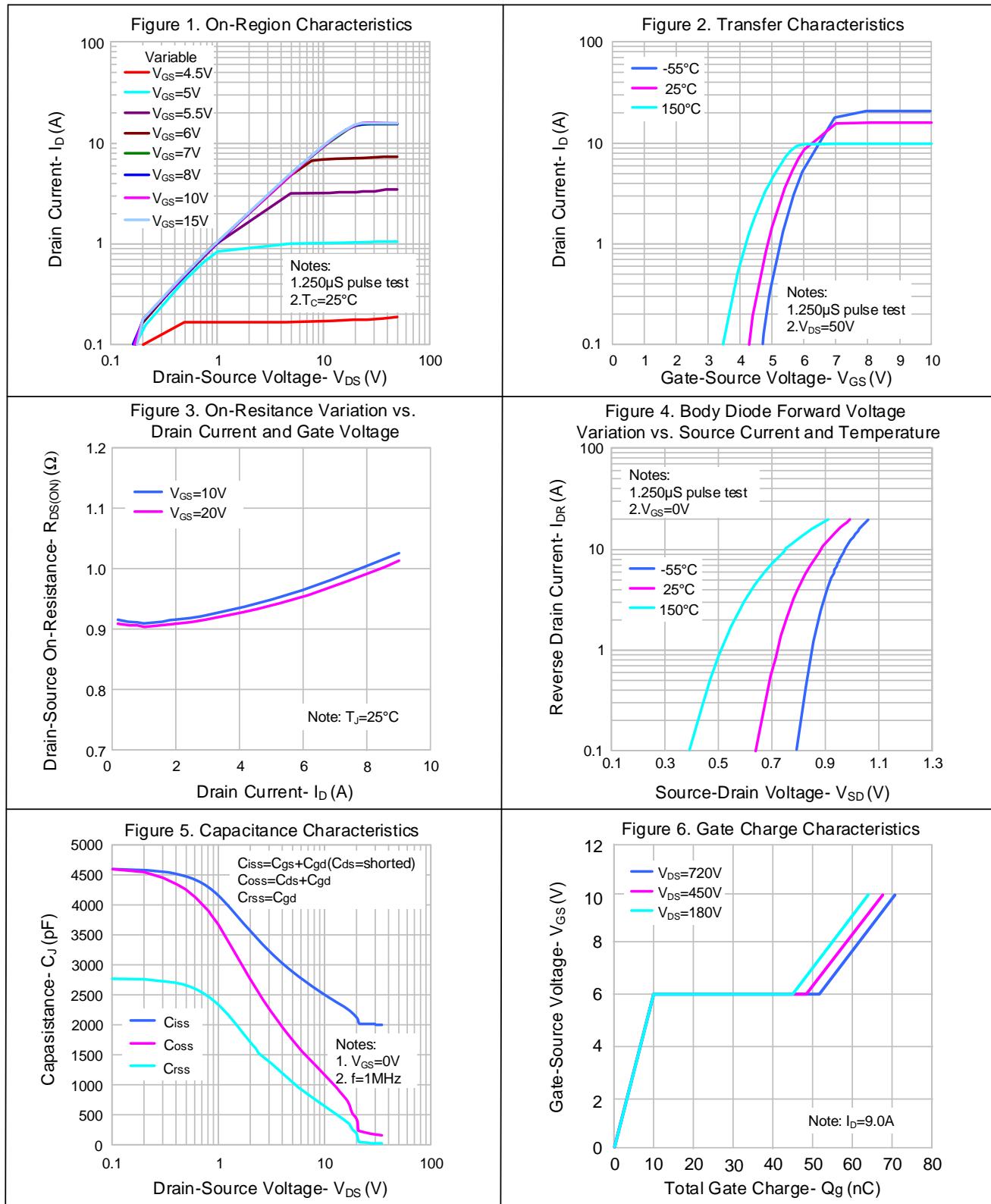
Notes:

1. $L=30mH, I_{AS}=7.70A, V_{DD}=100V, R_G=25\Omega$, starting $T_J=25^\circ C$;

2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;

3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

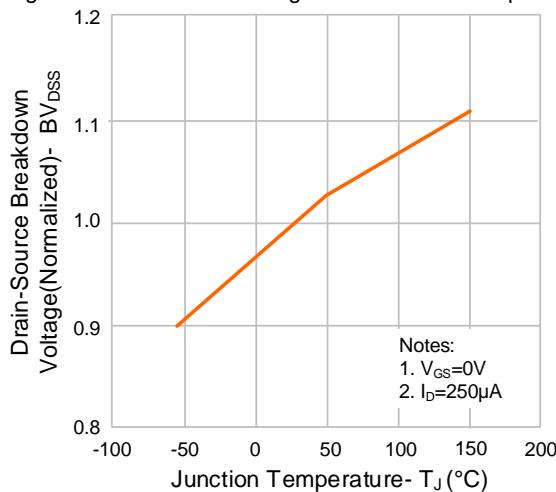


Figure 8. On-resistance Variation vs. Temperature

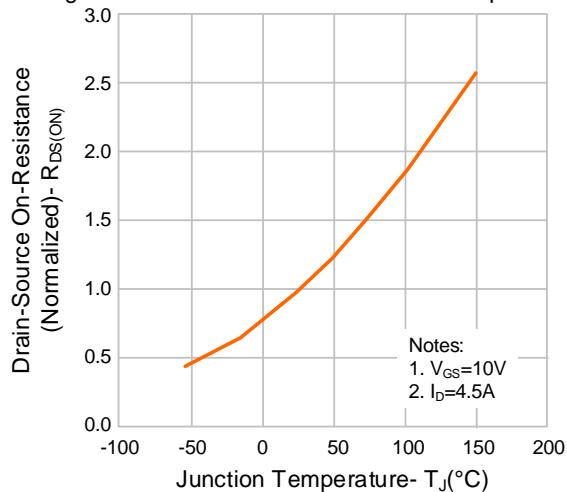


Figure 9. Max. Safe Operating Area

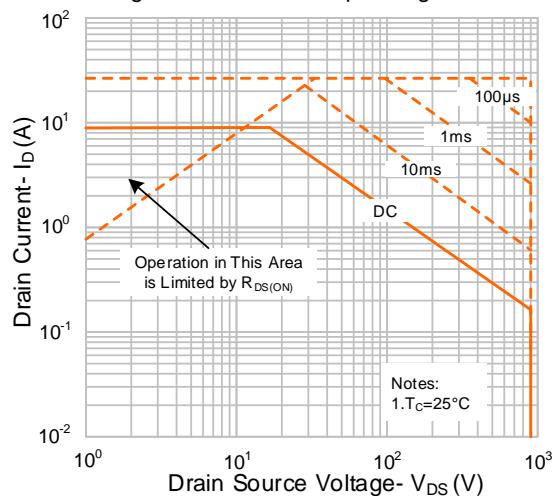
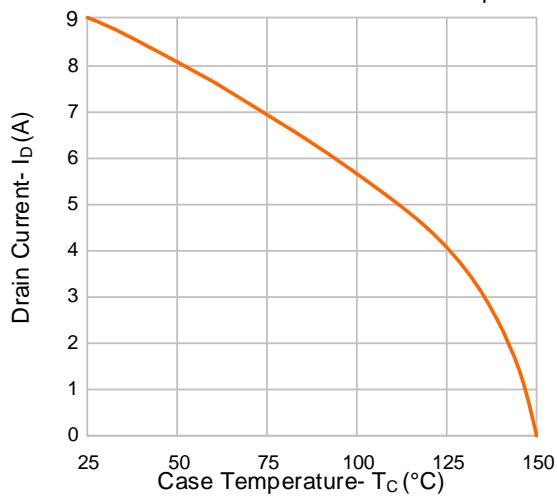
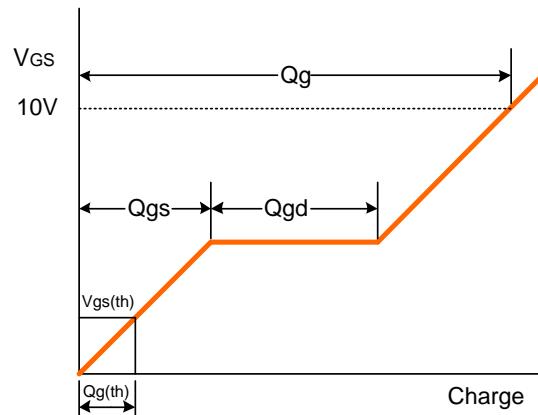
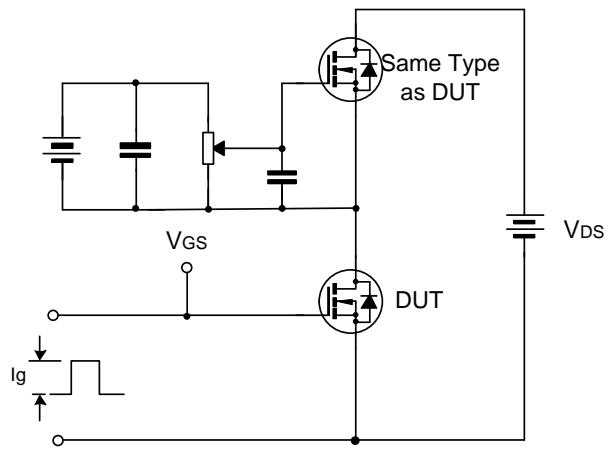


Figure 10. Maximum Drain Current vs. Case Temperature

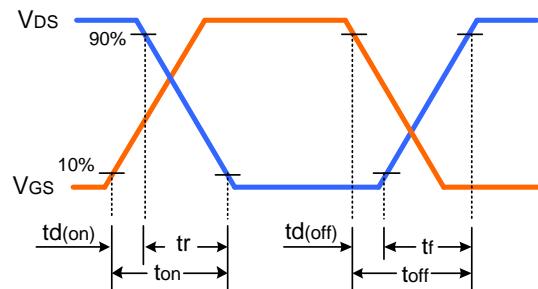
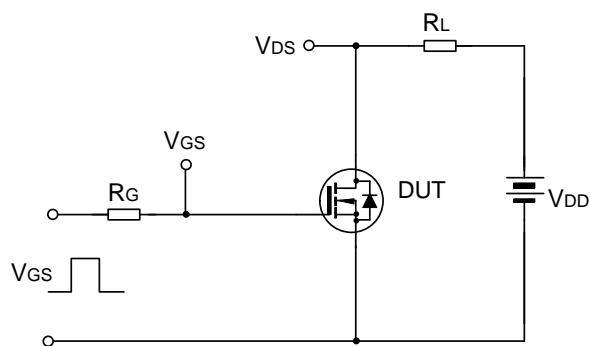


TYPICAL TEST CIRCUIT

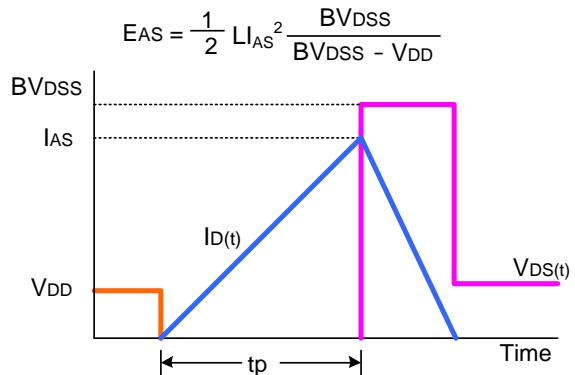
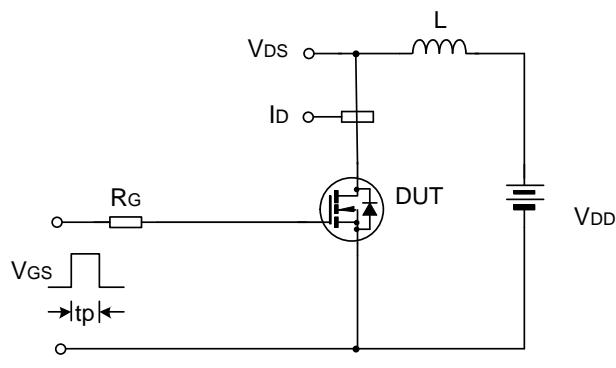
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-247-3L		UNIT: mm		
SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	4.80	5.00	5.20	
A1	2.21	2.41	2.59	
A2	1.85	2.00	2.15	
b	1.11	—	1.36	
b2	1.91	—	2.25	
b4	2.91	—	3.25	
C	0.51	—	0.75	
D	20.80	21.00	21.30	
E	15.50	15.80	16.10	
E2	4.40	5.00	5.20	
e	5.44 BSC			
L	19.72	19.92	20.22	
L1	—	—	4.30	
Q	5.60	5.80	6.00	
P	3.40	—	3.80	



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. The instructions are subject to change without notice!
2. Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.
3. Our products are consumer electronic products or the other civil electronic products.
4. When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.
5. It is strongly recommended to identify the trademark when buying our products. Please contact us if there is any question.
6. Product promotion is endless, our company will wholeheartedly provide customers with better products!
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Part No.: **SVF3878P7**

Document Type: **Datasheet**

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Rev.: **1.4**

Revision History:

1. Update package outline

Rev.: **1.3**

Revision History:

1. Update electrical and typical circuit diagrams
2. Modify the curve template and declaration
3. Update Hazardous Substance Control

Rev.: **1.2**

Revision History:

1. Update the package outline of TO-247-3L

Rev.: **1.1**

Revision History:

1. Add the MOS device notes.

Rev.: **1.0**

Revision History:

1. First release