

9A, 900V N-CHANNEL MOSFET

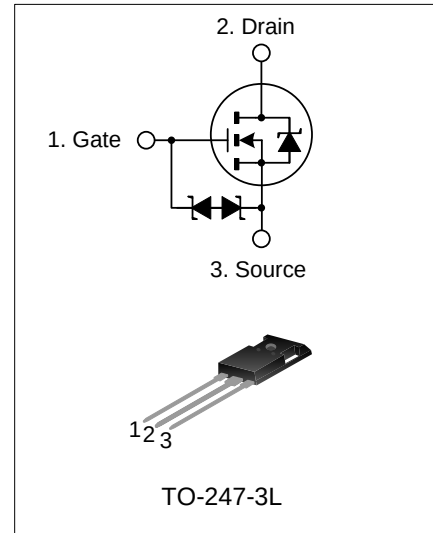
DESCRIPTION

SVF3878AP7 is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 9A, 900V, $R_{DS(on)}$ (typ.)=1.0 Ω @ V_{GS} =10V
- Low gate charge
- Low C_{rss}
- Fast switching
- Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF3878P7	TO-247-3L	3878A	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (unless otherwise noted, $T_C=25^\circ\text{C}$)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DS}	900	V
Gate-Source Voltage		V _{GS}	±30	V
Drain Current	T _C =25°C	I _D	9.0	A
	T _C =100°C		5.7	
Drain Current Pulsed		I _{DM}	27.0	A
Power Dissipation (T _C =25°C)		P _D	150	W
-Derate above 25°C			1.2	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	966	mJ
Operation Junction Temperature Range		T _J	-55~+150	°C
Storage Temperature Range		T _{stg}	-55~+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.83	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $T_c=25^{\circ}\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	900	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=900V, V_{GS}=0V$	--	--	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	± 10.0	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	3.0	V
On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.5A$	--	1.0	1.28	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	--	2009	--	pF
Output Capacitance	C_{oss}		--	208	--	
Reverse Transfer Capacitance	C_{rss}		--	47	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=400V, R_G=25\Omega, I_D=4.0A$ (Note2,3)	--	22	--	ns
Turn-on Rise Time	t_r		--	28	--	
Turn-off Delay Time	$t_{d(off)}$		--	84	--	
Turn-off Fall Time	t_f		--	30	--	
Total Gate Charge	Q_g	$V_{DD}=450V, V_{GS}=10V,$ $I_D=9.0A$ (Note 2,3)	--	68	--	nC
Gate-Source Charge	Q_{gs}		--	10	--	
Gate-Drain Charge	Q_{gd}		--	39	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	9.0	A
Pulsed Source Current	I_{SM}		--	--	27.0	
Diode Forward Voltage	V_{SD}	$I_S=9.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=9.0A, V_{GS}=0V,$ $dl/dt=100A/\mu S$ (Note2)	--	715	--	ns
Reverse Recovery Charge	Q_{rr}		--	6.5	--	μC

Notes:

1. $L=30mH, I_{AS}=7.70A, V_{DD}=100V, R_G=25\Omega$, starting $T_J=25^{\circ}\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

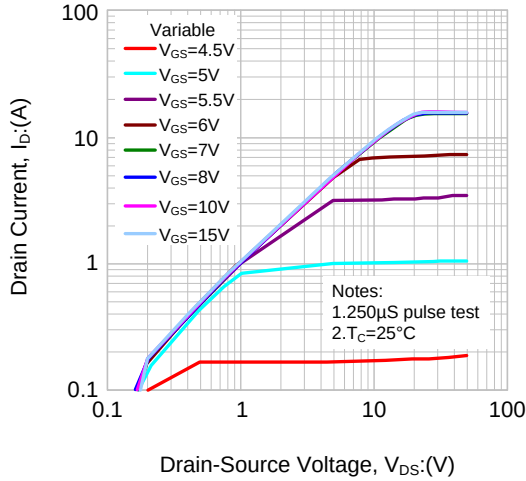


Figure 2. Transfer Characteristics

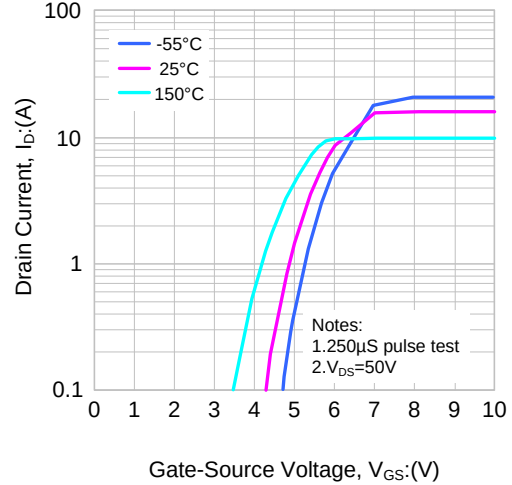


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

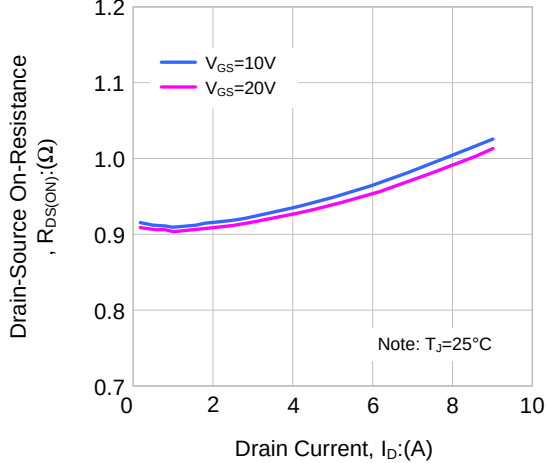


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

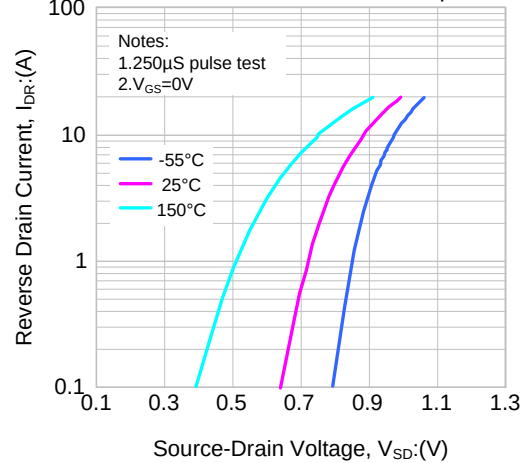


Figure 5. Capacitance Characteristics

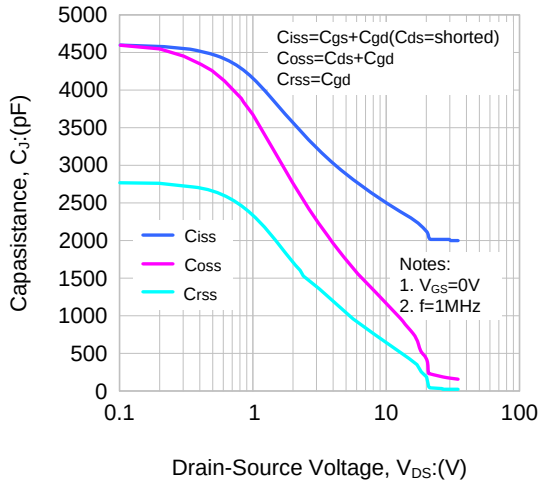
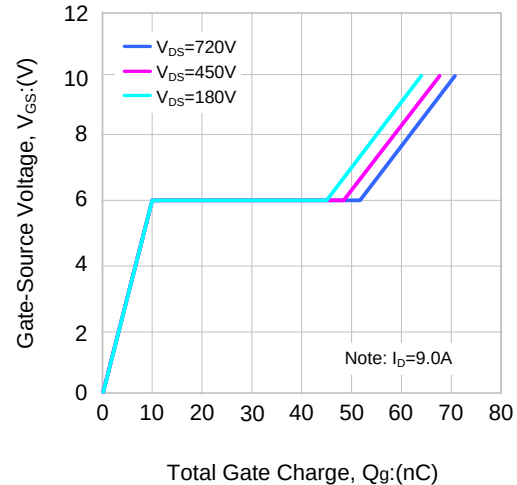


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

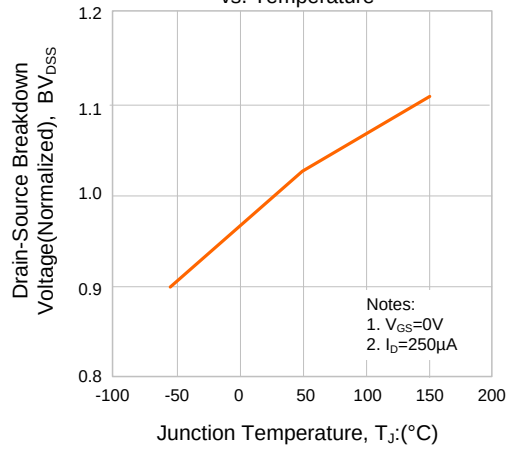


Figure 8. On-resistance Variation vs. Temperature

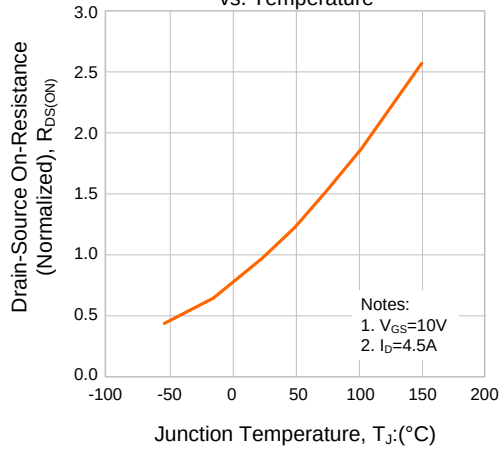


Figure 9. Max. Safe Operating Area

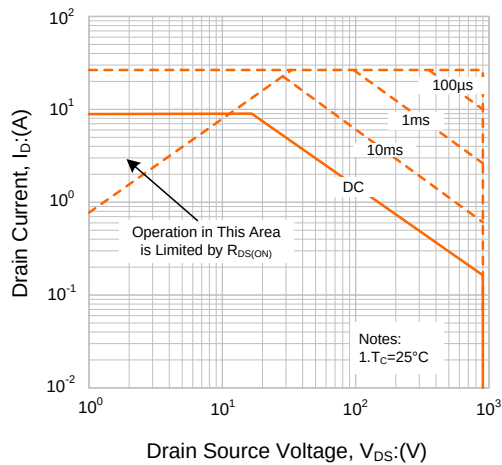
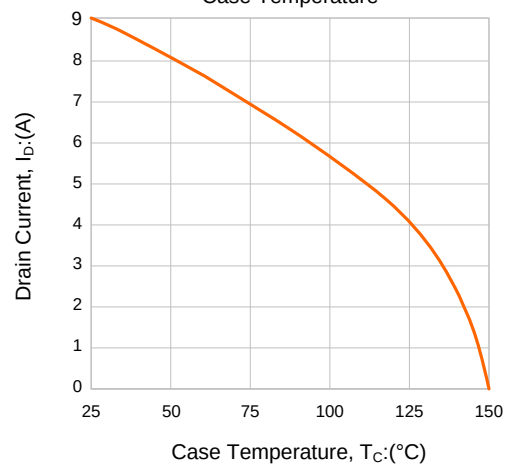
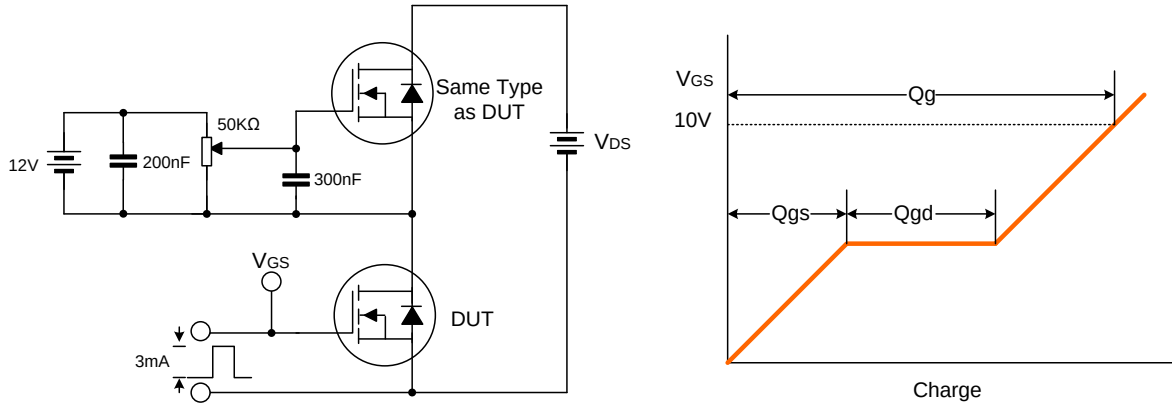


Figure 10. Maximum Drain Current vs. Case Temperature

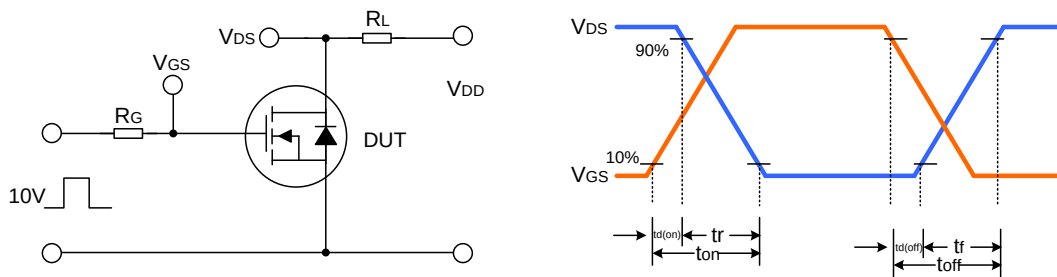


TYPICAL TEST CIRCUIT

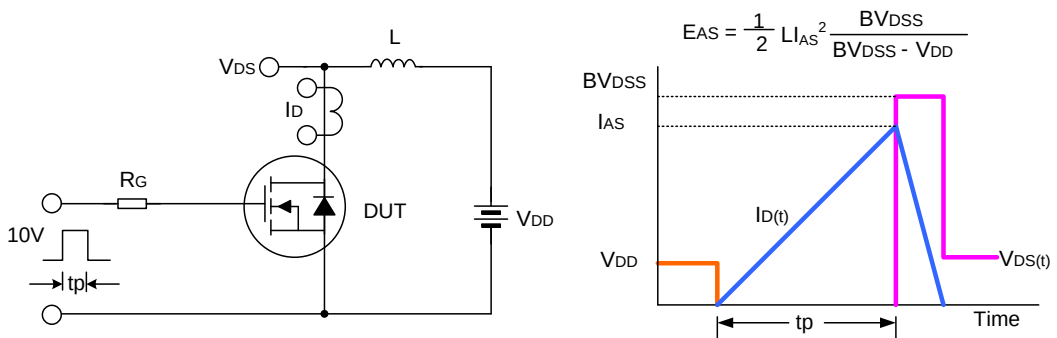
Gate Charge Test Circuit & Waveform



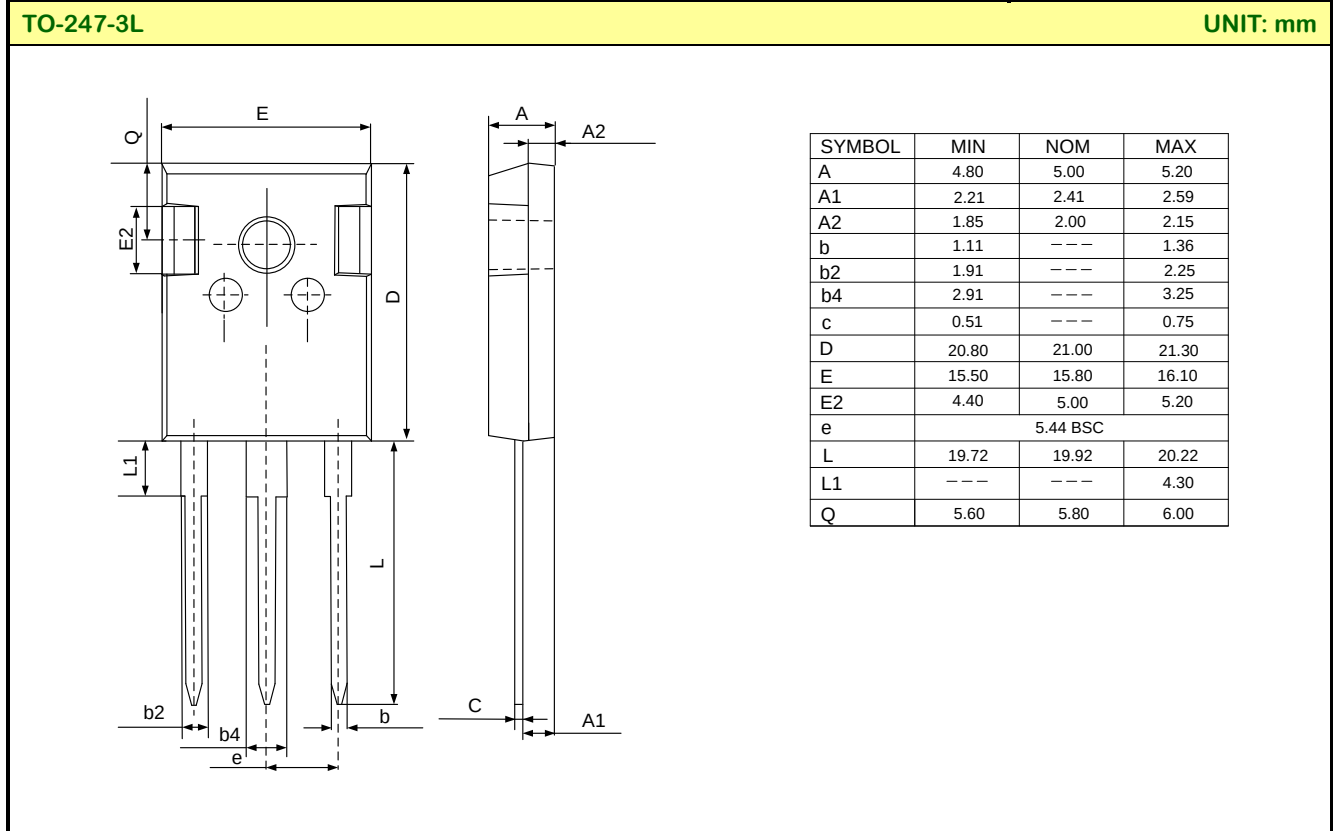
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
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Part No.:	SVF3878AP7	Document Type:	Datasheet
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Rev.: 1.1

Revision History:

1. Update the package outline of TO-247-3L
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Rev.: 1.0

Revision History:

1. First release
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