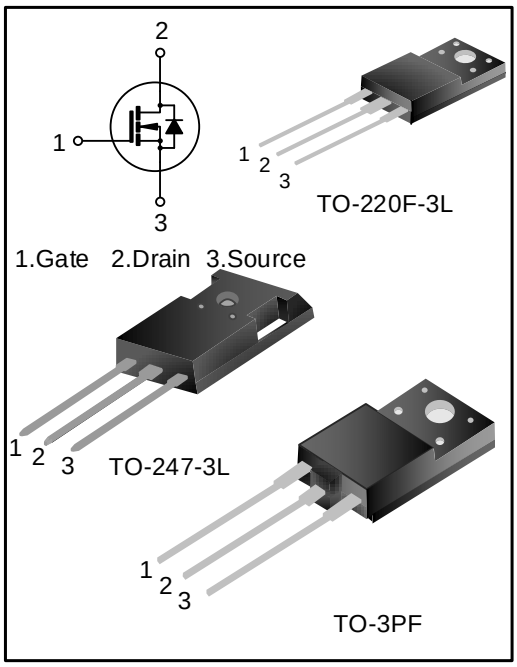
4A, 1500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF4N150PF(P7)(F) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in power supplies.



FEATURES

- 4A, 1500V, $R_{DS(on)(typ)}$=5.0Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF4N150PF	TO-3PF	4N150	Pb free	Tube
SVF4N150P7	TO-247-3L	4N150P7	Pb free	Tube
SVF4N150F	TO-220F-3L	SVF4N150F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings			Unit
			SVF4N150PF	SVF4N150P7	SVF4N150F	
Drain-Source Voltage		V_{DS}	1500			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	4.0			A
	T_C=100°C		2.5			
Drain Current Pulsed		I_{DM}	16			A
Power Dissipation(T_C=25°C)		P_D	73	160	39	W
-Derate above 25°C			0.49	1.28	0.3	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	485			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF4N150PF	SVF4N150P7	SVF4N150F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.7	0.78	3.17	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	50	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	1500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=1500V, V_{GS}=0V	--	--	10.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±500	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	3.0	--	5.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.3A	--	5.0	6.5	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	1034	--	pF
Output Capacitance	C_{oss}		--	91	--	
Reverse Transfer Capacitance	C_{rss}		--	12	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=750V， I_D=4A， R_G=25Ω (Note2,3)	--	25	--	ns
Turn-on Rise Time	t_r		--	51	--	
Turn-off Delay Time	$t_{d(off)}$		--	86	--	
Turn-off Fall Time	t_f		--	46	--	
Total Gate Charge	Q_g	V_{DS}=1200V, I_D=4A, V_{GS}=10V (Note 2,3)	--	40	--	nC
Gate-Source Charge	Q_{gs}		--	8.7	--	
Gate-Drain Charge	Q_{gd}		--	23	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 2)	--	373	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.4	--	μC

Notes:

1. L=79mH, I_{AS}=3.4A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature..

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

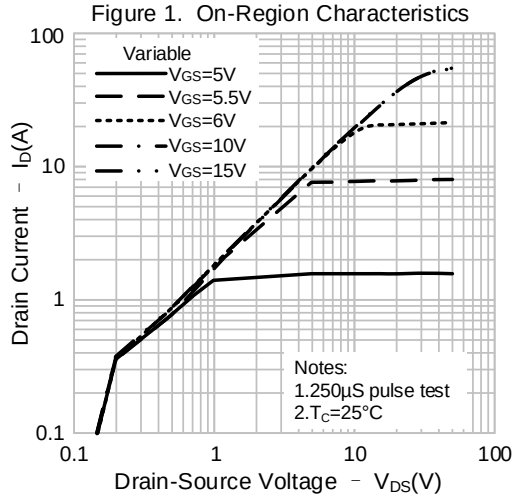


Figure 2. Transfer Characteristics

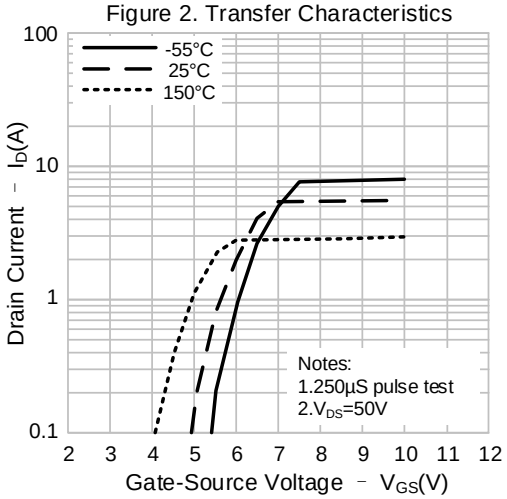


Figure 3. On-Resistance Variation vs. Drain Current

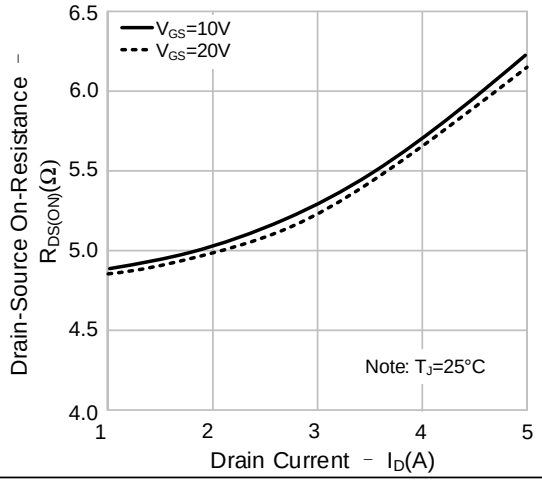


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

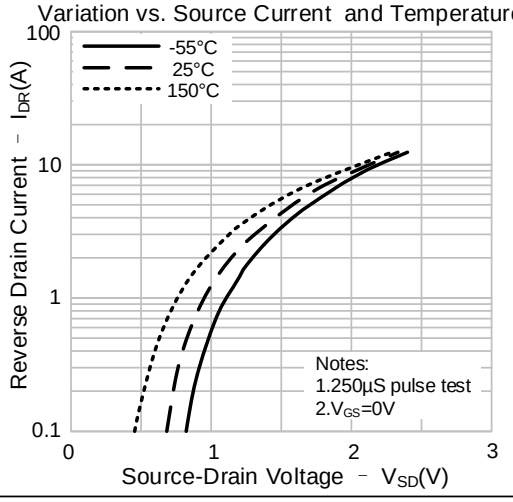


Figure 5. Capacitance Characteristics

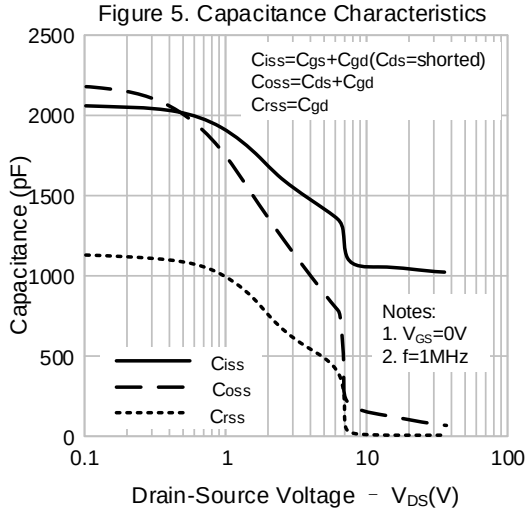
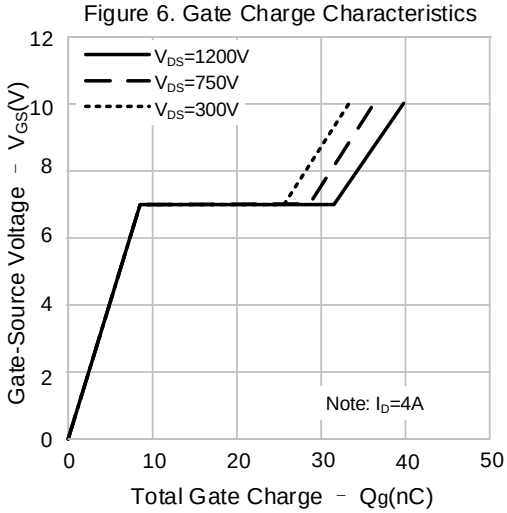


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

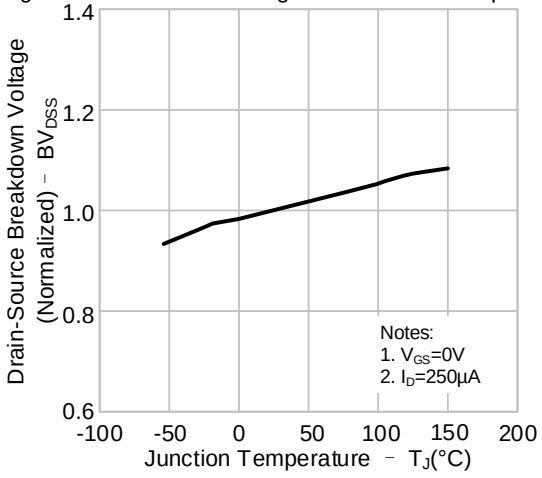


Figure 8. On-Resistance Variation vs.Temperature

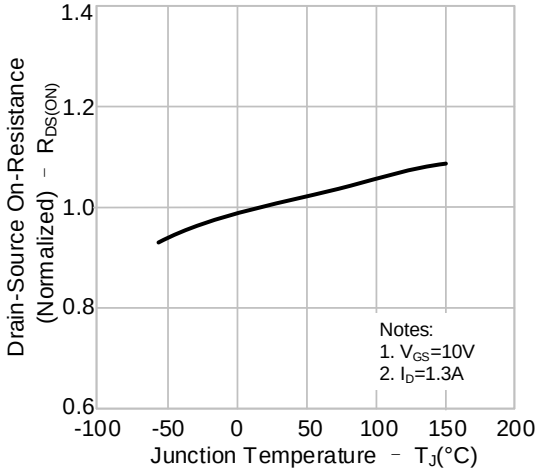


Figure 9-1. Max. Safe Operating Area(SVF4N150PN)

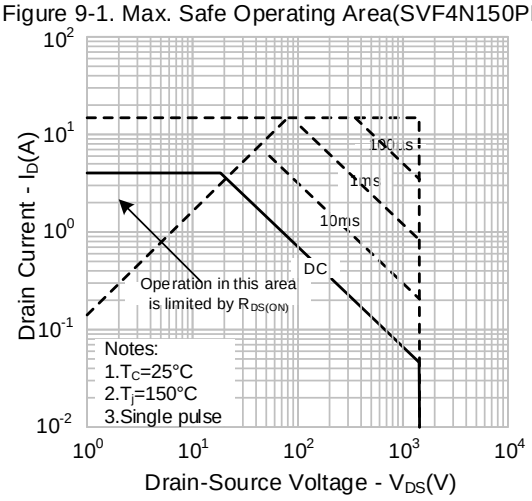


Figure 9-2. Max. Safe Operating Area(SVF4N150P7)

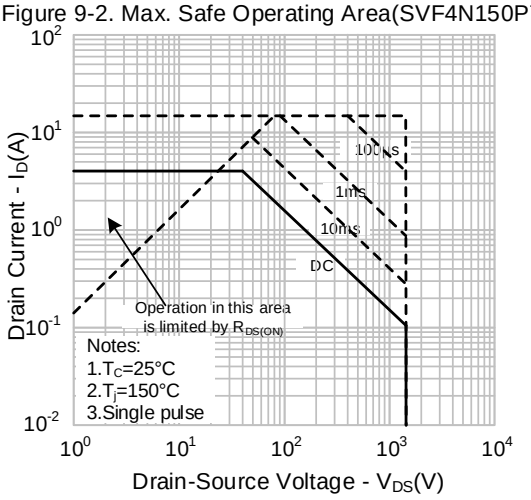


Figure 9-3. Max. Safe Operating Area(SVF4N150F)

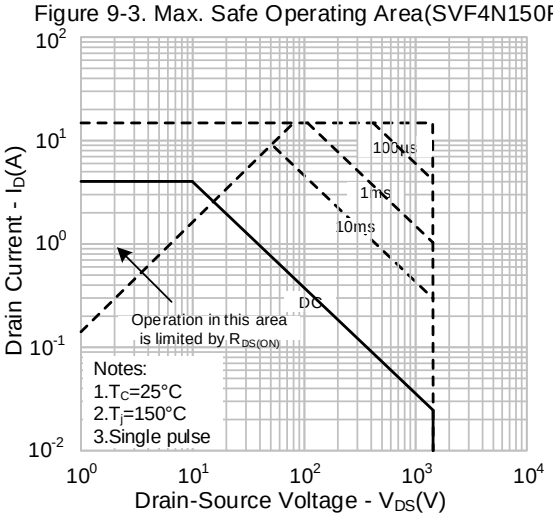
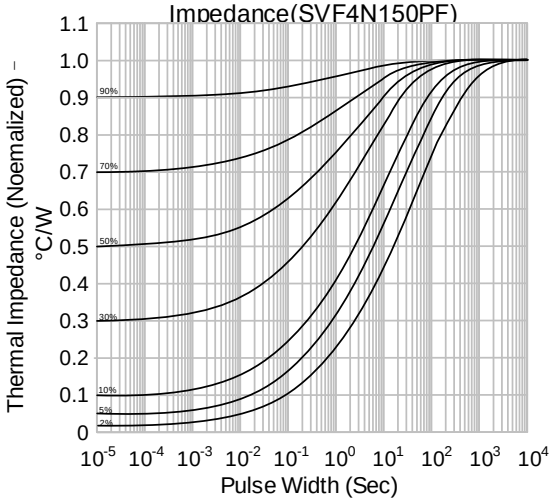


Figure 10-1. Transient Thermal Impedance(SVF4N150PF)



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 10-2. Transient Thermal Impedance(SVF4N150P7)

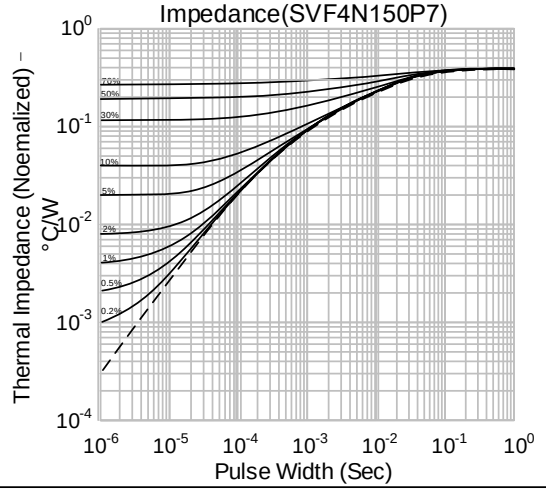
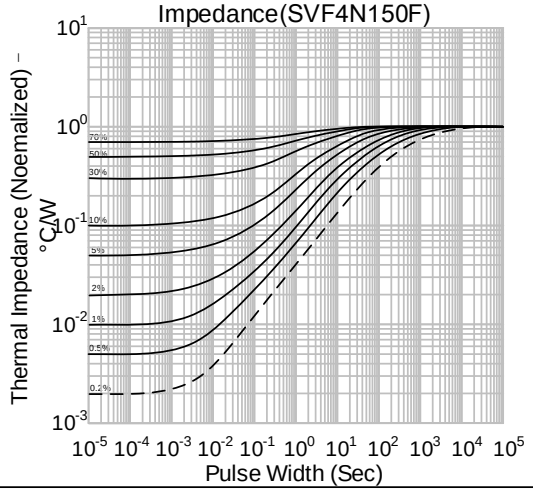
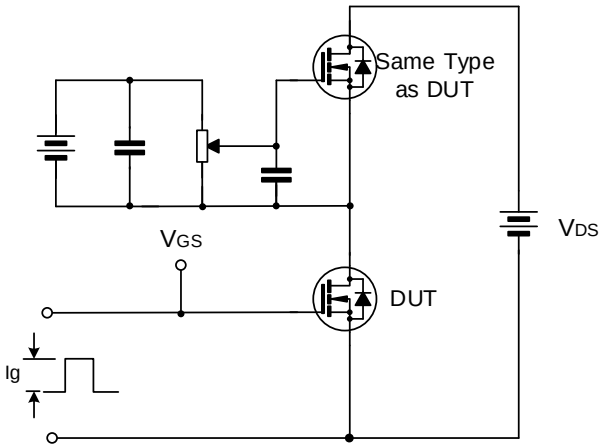


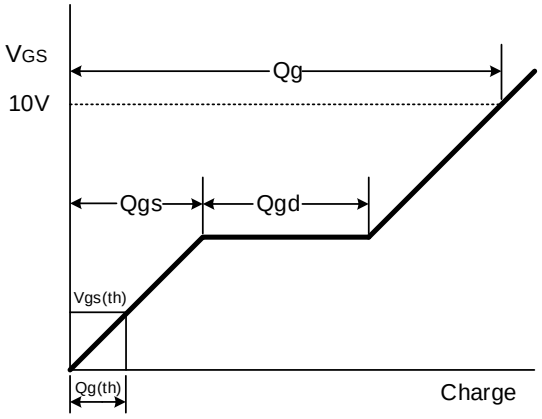
Figure 10-3. Transient Thermal Impedance(SVF4N150F)



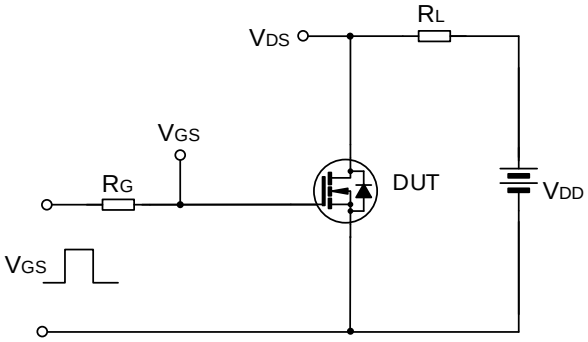
TYPICAL TEST CIRCUIT

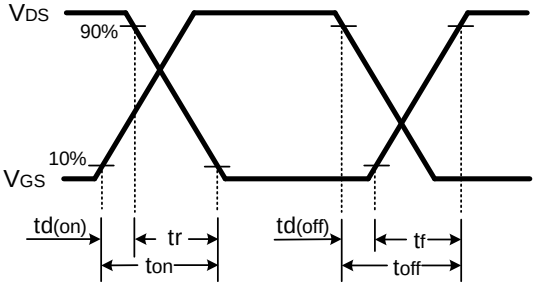
Gate Charge Test Circuit & Waveform



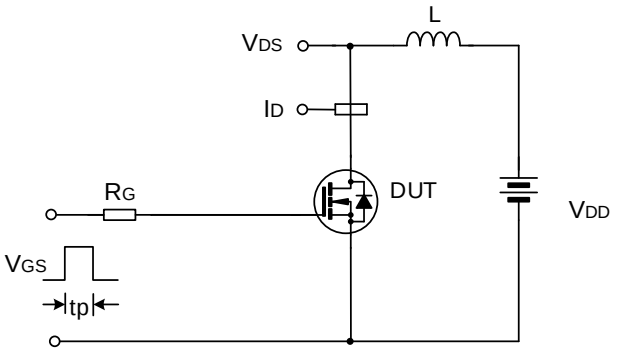


Resistive Switching Test Circuit & Waveform

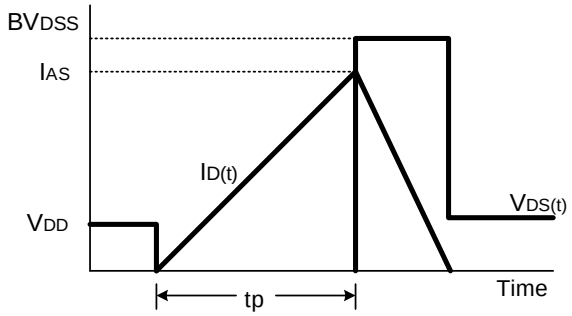




Unclamped Inductive Switching Test Circuit & Waveform



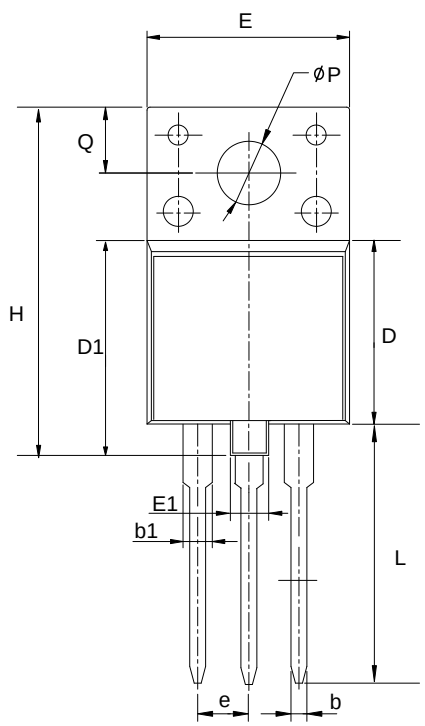
$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

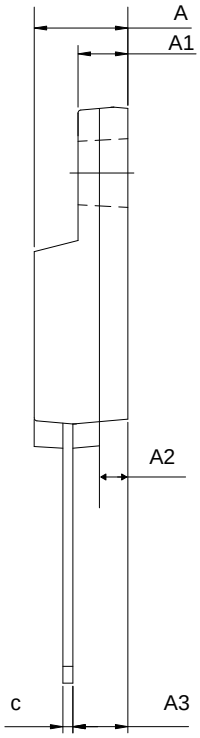


PACKAGE OUTLINE

TO-3PF

UNIT: mm

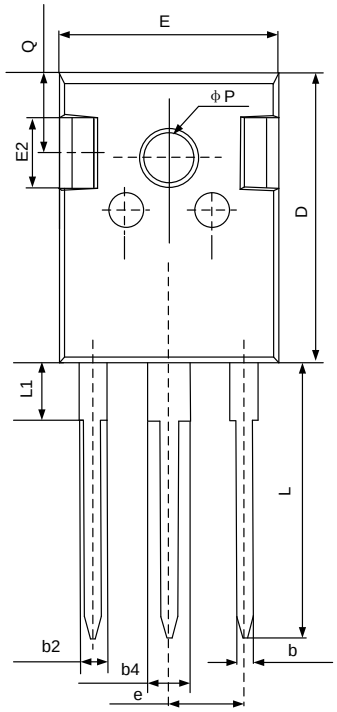


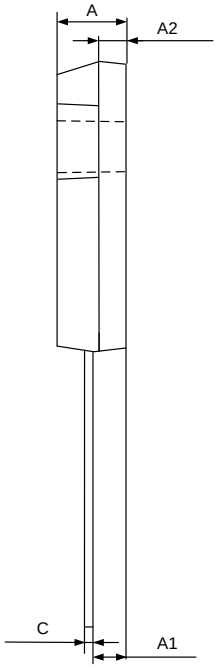


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	5.20	5.50	5.80
A1	2.80	3.00	3.20
A2	1.70	2.00	2.30
A3	3.00	3.40	3.80
b	0.65	0.80	0.95
b1	1.80	2.00	2.20
c	0.70	0.90	1.10
D	14.30	—	15.50
D1	16.30	—	17.70
E	15.30	15.50	15.70
E1	3.80	4.00	4.20
e	5.15	5.45	5.75
H	26.10	26.50	26.90
L	18.50	—	19.70
ØP	3.40	3.60	3.80
Q	4.30	4.50	4.70

TO-247-3L

UNIT: mm

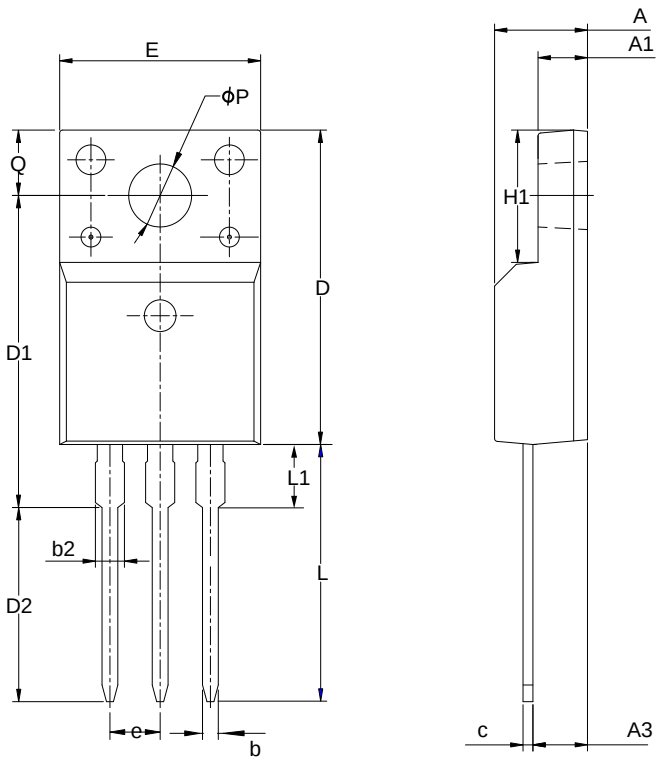




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	–	1.36
b2	1.91	–	2.25
b4	2.91	–	3.25
c	0.51	–	0.75
D	20.80	21.00	21.30
E	15.50	15.80	16.10
E2	4.40	5.00	5.20
e	5.44 BSC		
L	19.72	19.92	20.22
L1	–	–	4.30
Q	5.60	5.80	6.00
P	3.40	—	3.80

PACKAGE OUTLINE(CONTINUED)

TO-220F-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
2. Customers should obtain the latest relevant information when purchasing and should verify whether such information is latest and complete. Please read this instruction and application manual and related materials carefully before using products, including the circuit operation precautions, etc.
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7. Please use and apply product in compliance with all applicable laws and regulations, including but not limited to trade control regulations etc. The product is civil electronic product, please do not use it in non-civil fields.
8. Product promotion is endless, our company will wholeheartedly provide customers with better products!
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Rev.: 1.7

Revision History:

1. Delate TO-263-2L package
2. Update typical characteristics

Rev.: 1.6

Revision History:

1. Update the important notice
2. Update the package outline of TO-263-2L

Rev.: 1.5

Revision History:

1. Add TO-263-2L
2. Update Fig 9-2
3. Update the template of datasheet

Rev.: 1.4

Revision History:

1. Update the package outline of TO-3PF
2. Update the package outline of TO-247-3L

Rev.: 1.3

Revision History:

1. Add the package outline of TO-220F-3L

Rev.: 1.2

Revision History:

1. Add the package outline of TO-247-3L

Rev.: 1.1

Revision History:

1. Modify the ID=6.5A to 2.0A of Fig.8:

Rev.: 1.0

Revision History:

1. First release